JADARD

JD79661AA

Data Sheet

All-in-one driver with
TCON for Color application

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 2-bit output per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows to generate the source output voltage VSP_0/VSN_0(+/-15V),VSP_1/VSPL_0/VSPL_1/VSN_1 (+/-3V~+/-15V) and VGP/VGN(+/-20V, +/-17V, +/-15V, +/-10V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

2. FEATURES

- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 176x296)
- Support source & gate driver function:
  - 176 Outputs source driver with 2-bit black/white/red/yellow per pixel:
    - Output dynamic range(Voltage step:100mV):
      - Mode 0: 0V & VSP_0(+15V) & VSN_0(-15V) & VSPL_0(+3V~+15V)
      - Mode 1: 0V & VSP_1 (+3V ~ +15V) & VSN_1(-3V ~ -15V) & VSPL_1 (+3V ~ +15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 296 Output gate driver:
    - Output dynamic range: VGP and VGN(+/-20V, +/-17V, +/-15V, +/-10V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (7-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: 176x 296 x 2 bit SRAM
- Built in temperature sensor:
  - On-Chip: -25 ^{o}C ~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V

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- 6K-byte MTP for LUT, User command
- Partial update
- Support cascade
- Package-COG

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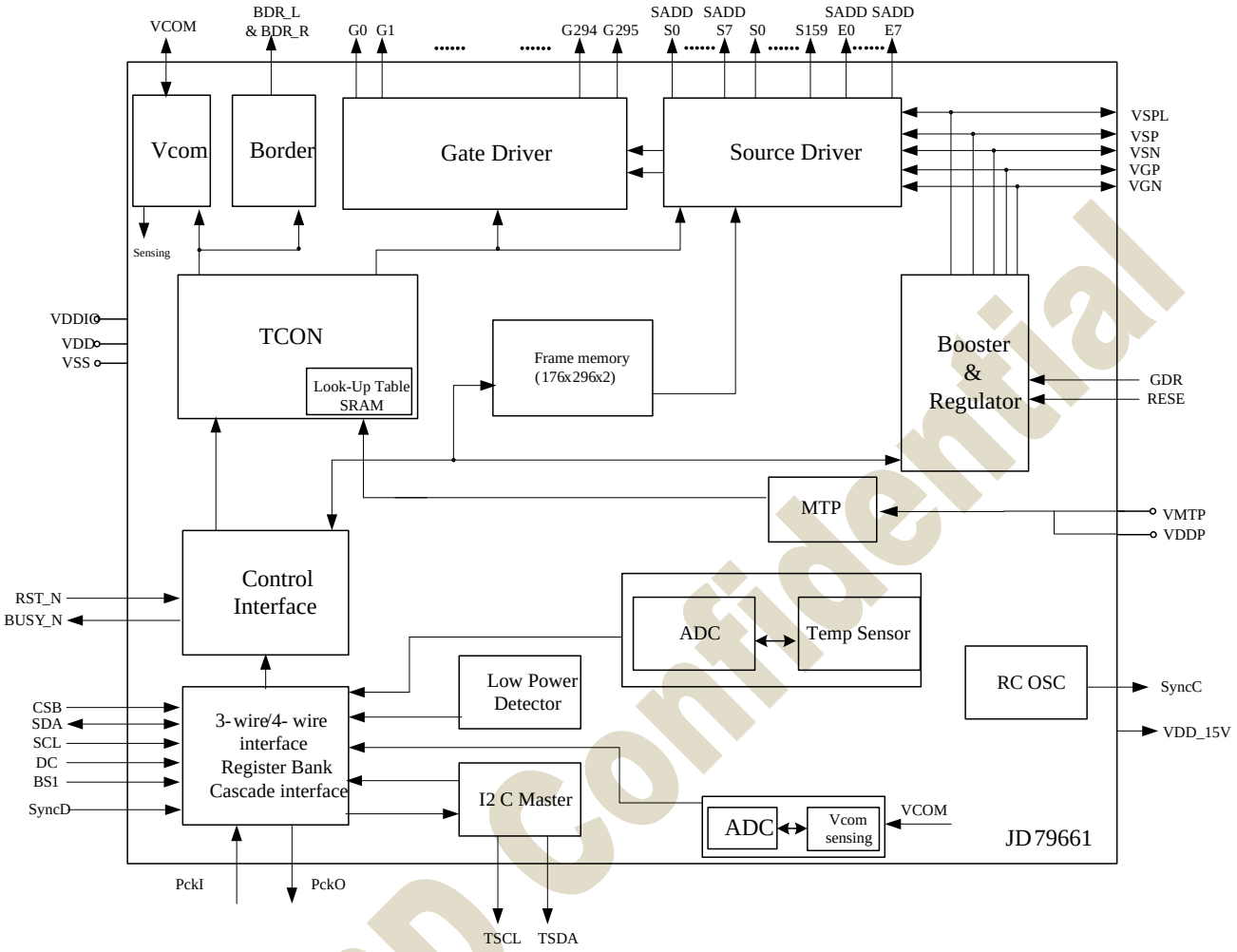
3. BLOCK DIAGRAM



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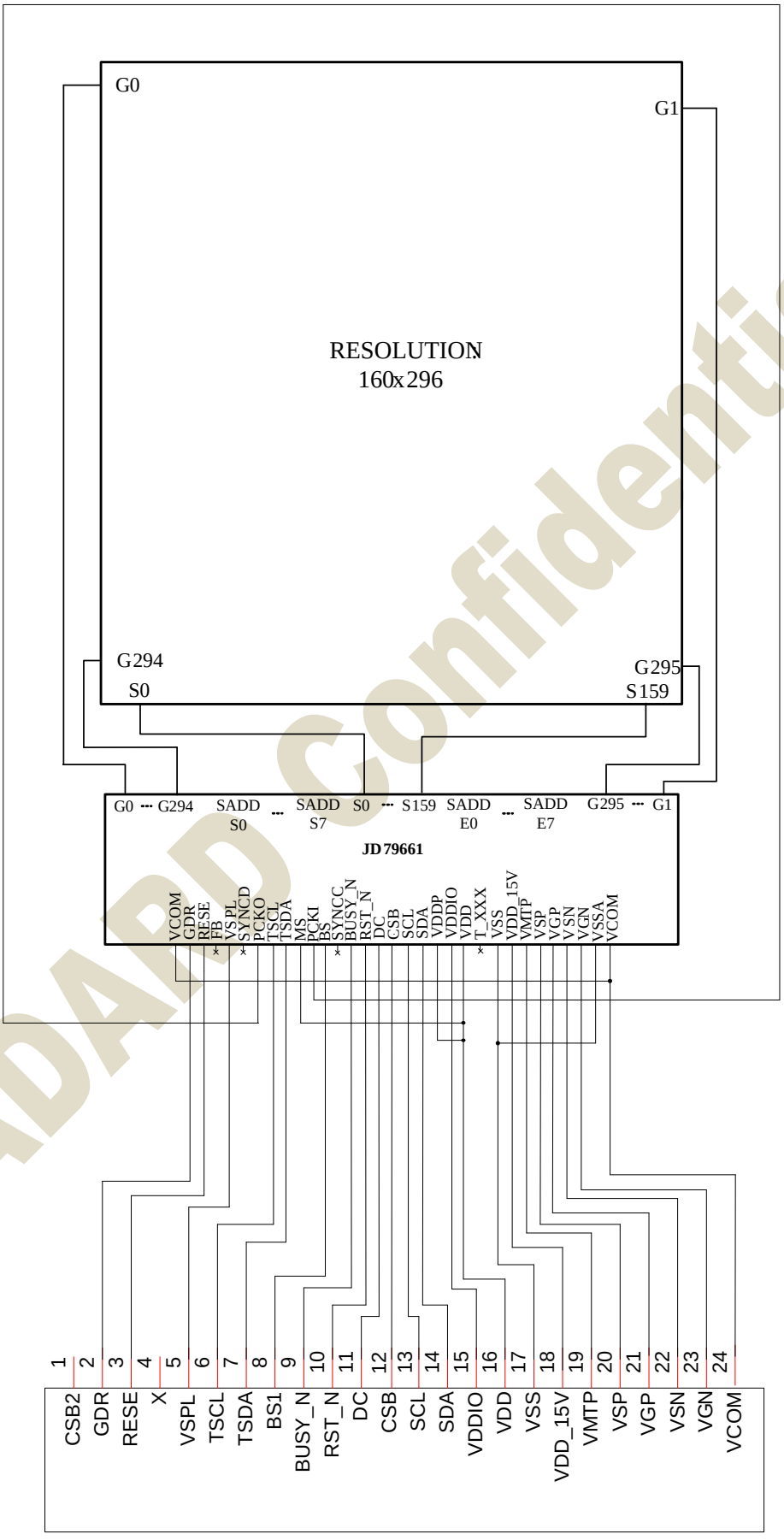
Normal type 1 (source resolution below 160ch.)



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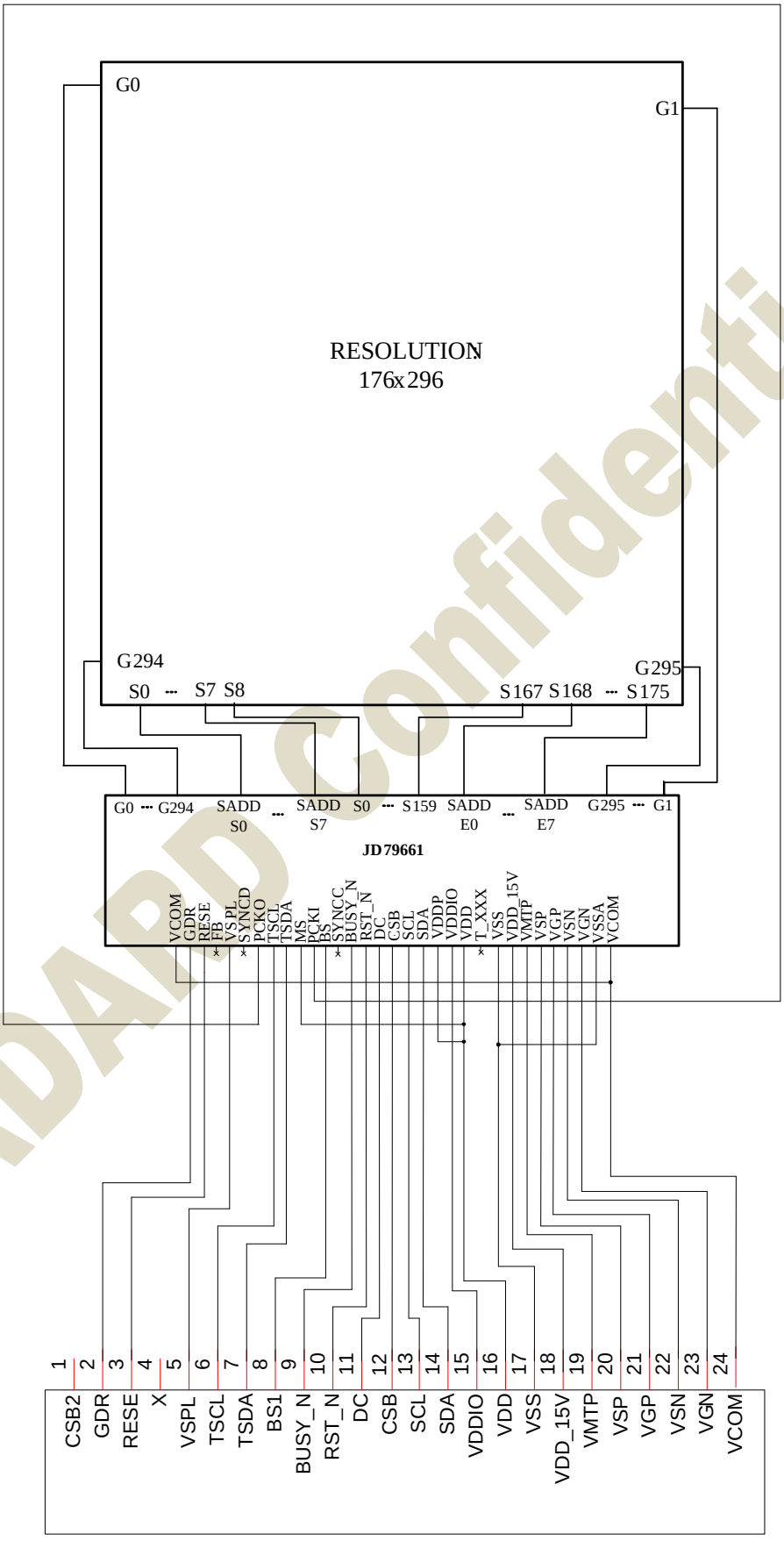
Normal type 2 (source resolution 176ch.)



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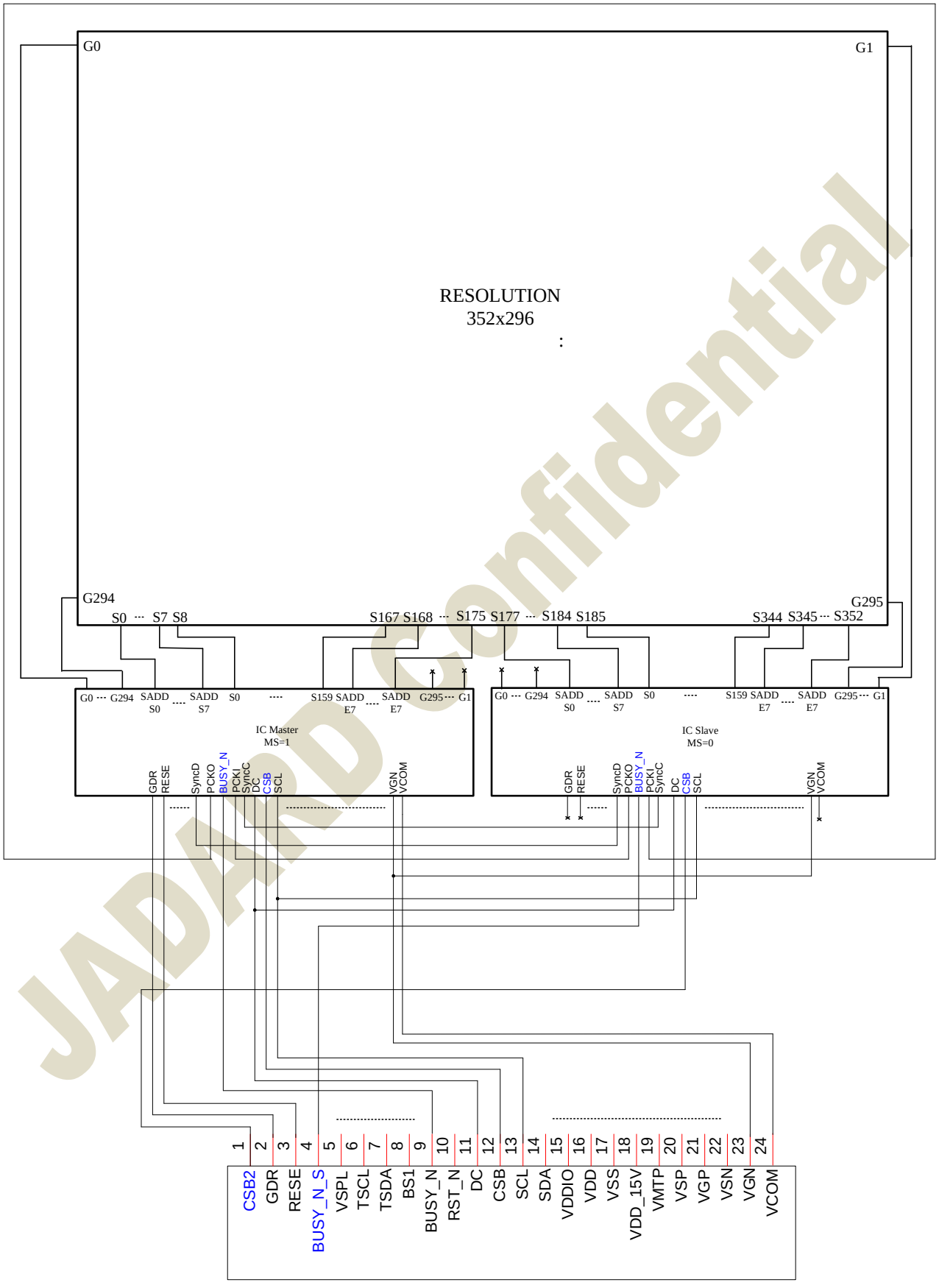
Cascade type



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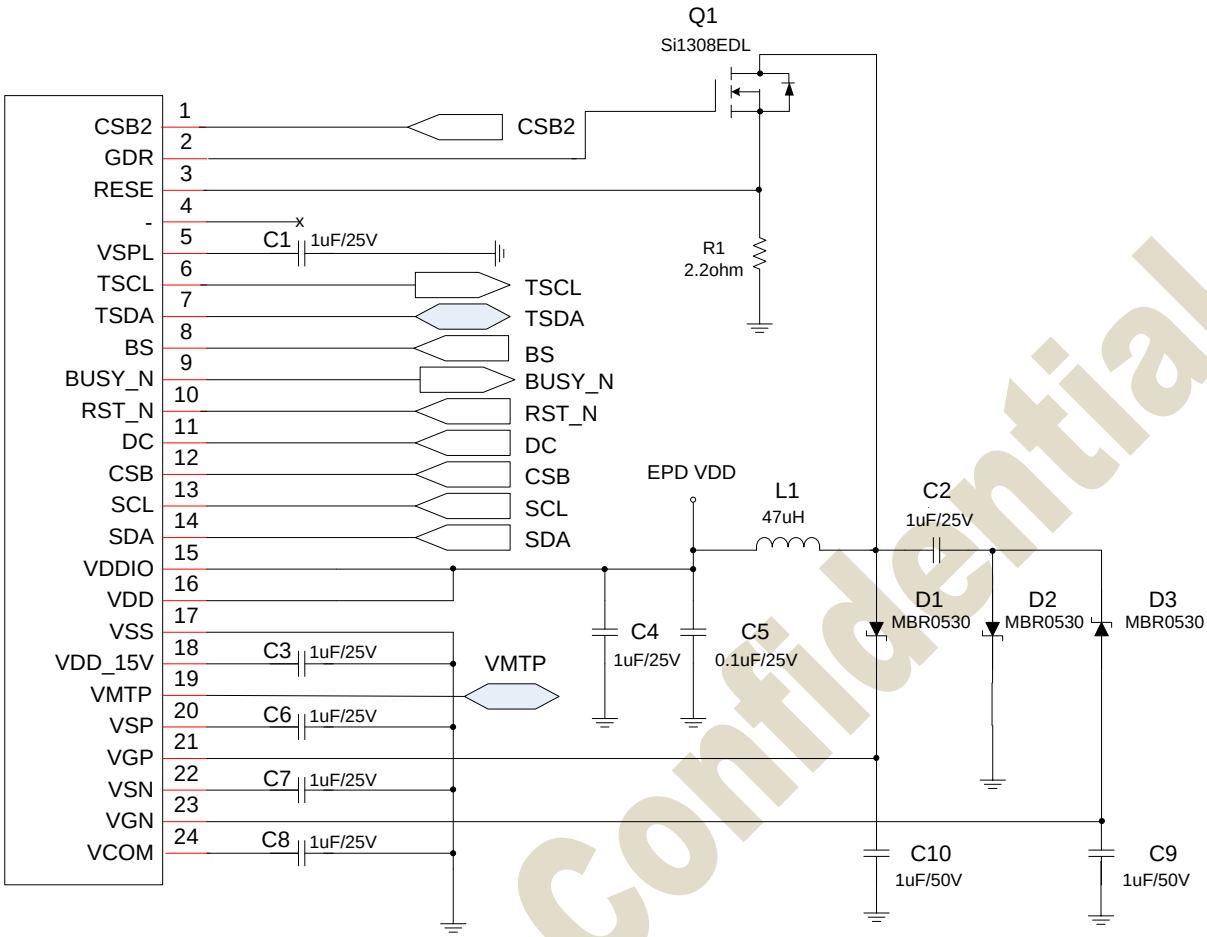
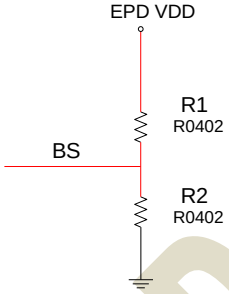
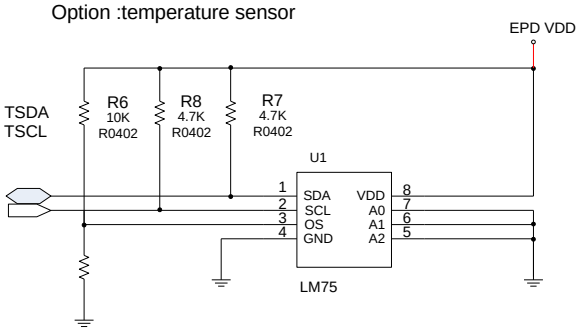
4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K



Reference table of the device:

Device no.	Value	Reference
C1,C2,C3, C4, C6, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C9, C10	1uF	0603, X5R/X7R, voltage rating : 50V
C5	0.1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ

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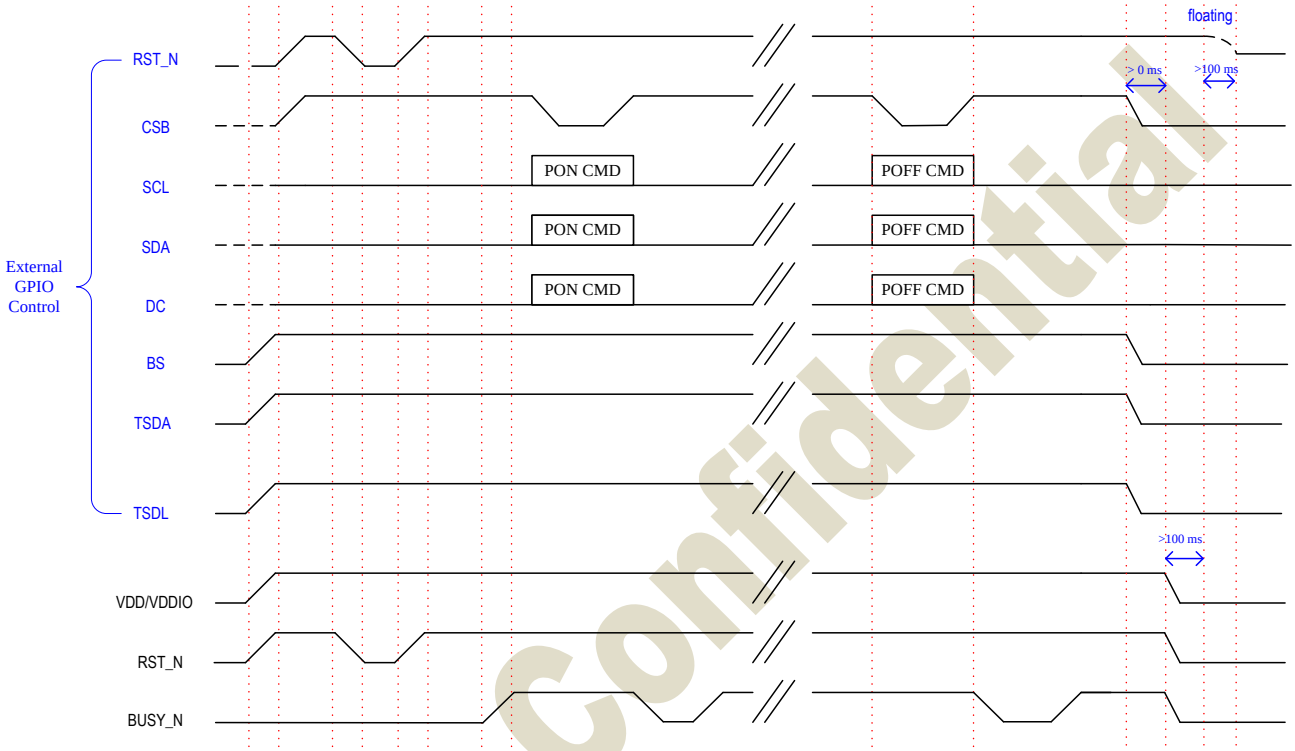
D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

4.1 External GPIO Control



Note:
TSDA: I^{2}C data for external temperature sensor
TSCL: I^{2}C clock for external temperature sensor
(I^{2}C interface need external pull high resistance. Pull low or floating If not used.)

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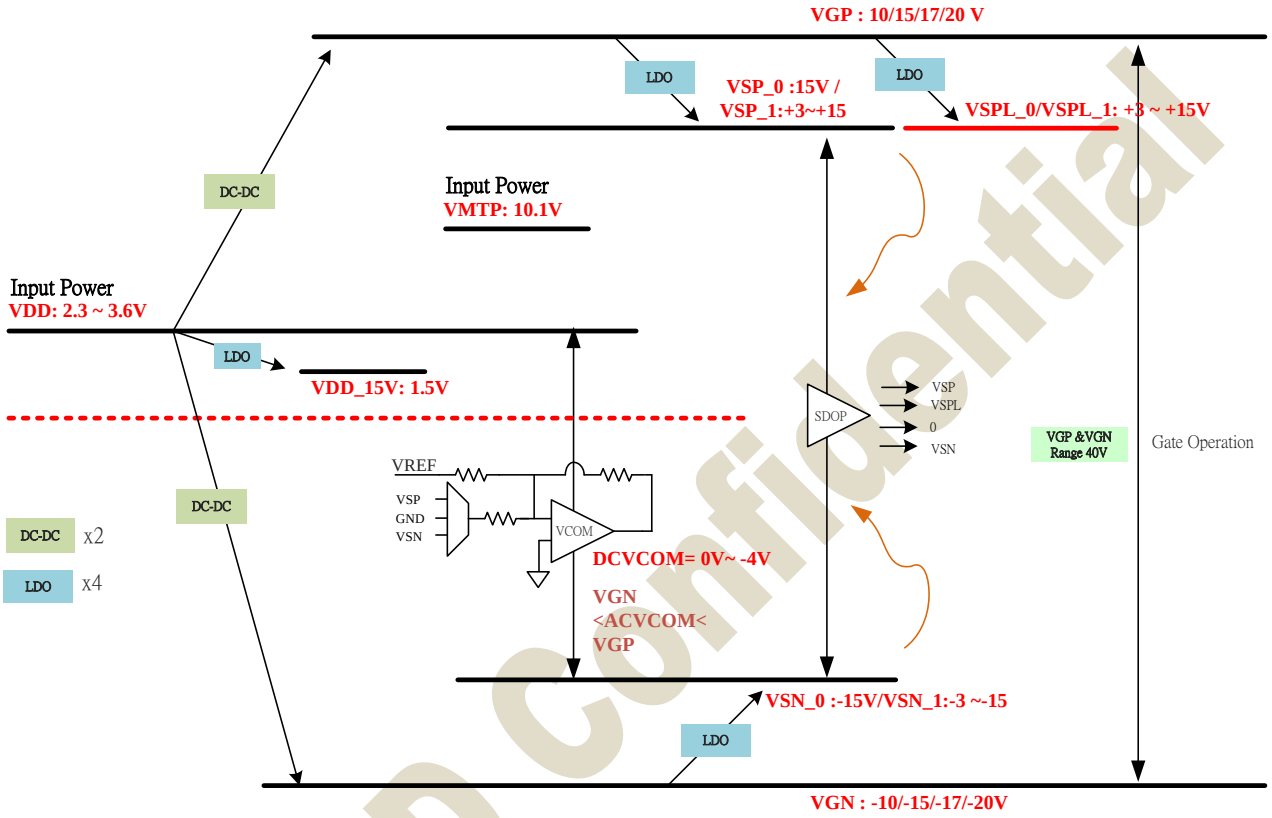
5. APPLICATION POWER CIRCUIT

5.1 Power Generation



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6. PIN DESCRIPTION

6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. (normal pull high) When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	O	Type1	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
TSDA	I/O	Type 4	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[159:0]	O	-	Source driver output signals.
S_ADDS/E[7:0]	O	-	Source driver output signals.
G[295:0]	O	-	Gate driver output signals..
Border			
VBD[4:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) V 2. (15 +(- VCM_DC)) V or (-15 +(- VCM_DC)) V 3. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGP	P	Type 5	Positive gate voltage
VGN	P	Type 4	Negative gate voltage.
VSP	P	Type 1	Positive source voltage

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Pin Name	Pin Type	I/O Structure	Description
VSN	P	Type 1	Negative source voltage.
VSPL	P	Type 1	Positive source voltage
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VMTP	P	-	MTP program power (10.1V)
Reserved Pins			
TP [21:0]	I/O	-	Test pin.Leave open or pull gnd if it is not used.
SyncD	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or gnd if it is not used.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

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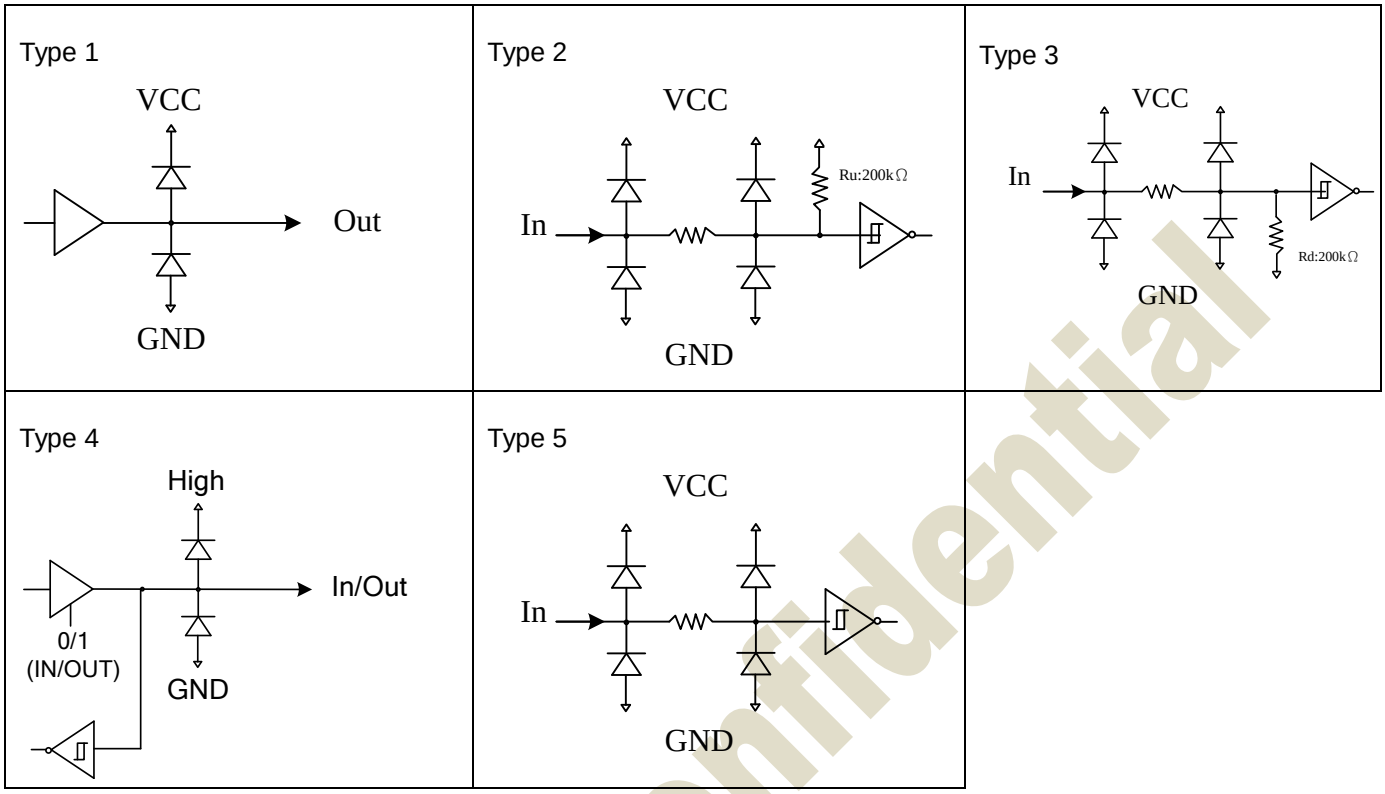
6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGP	5ohm	TSCL	100ohm
VGN	5ohm	BUSY_N	100ohm
VSP	5ohm	BS	100ohm
VSN	5ohm	RESE	5ohm
VSPL	5ohm	GDR	5ohm
VMTP	5ohm	SDA	100ohm
VDD_18V	5ohm	SCL	100ohm
VSSA	5ohm	CSB	100ohm
VDDIO	5ohm	DC	100ohm
VSS	5ohm	RST_N	100ohm
VDDP	5ohm	SyncD	100ohm
VDD	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
TP [21:0]	100ohm	PCKO	100ohm

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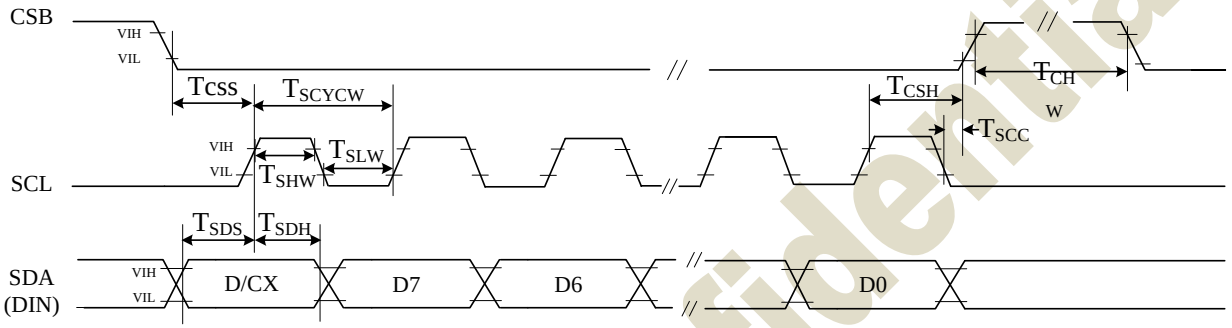
7. SPI COMMAND DESCRIPTION

JD79661 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

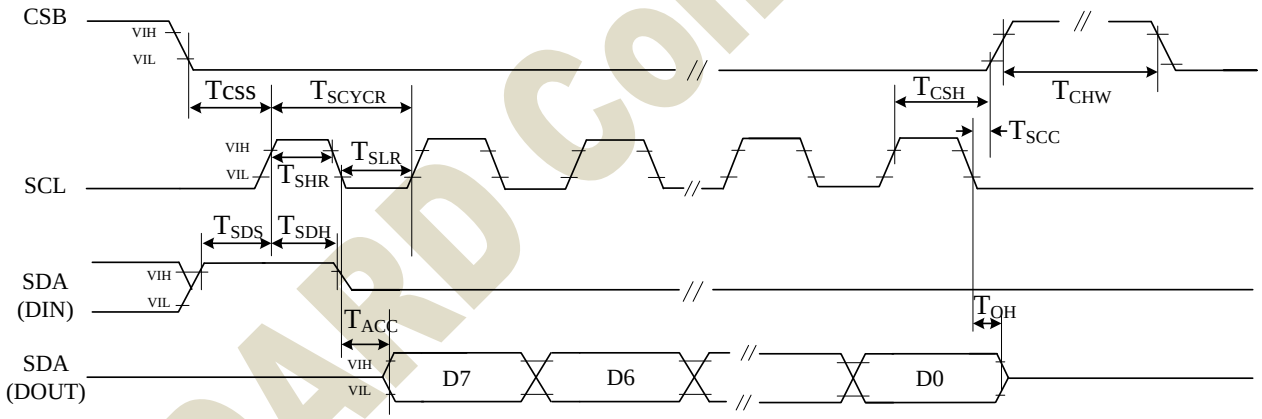
JD79661 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

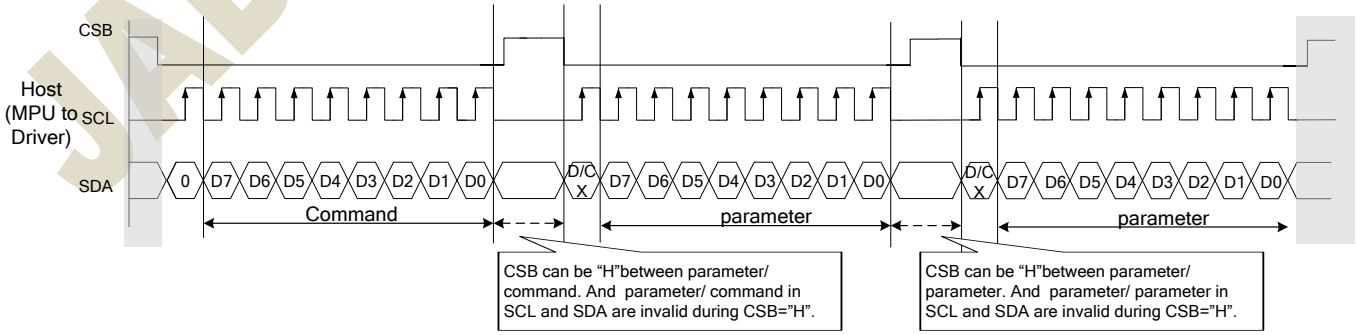
7.1 “3-Wire” Serial Port Interface



3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



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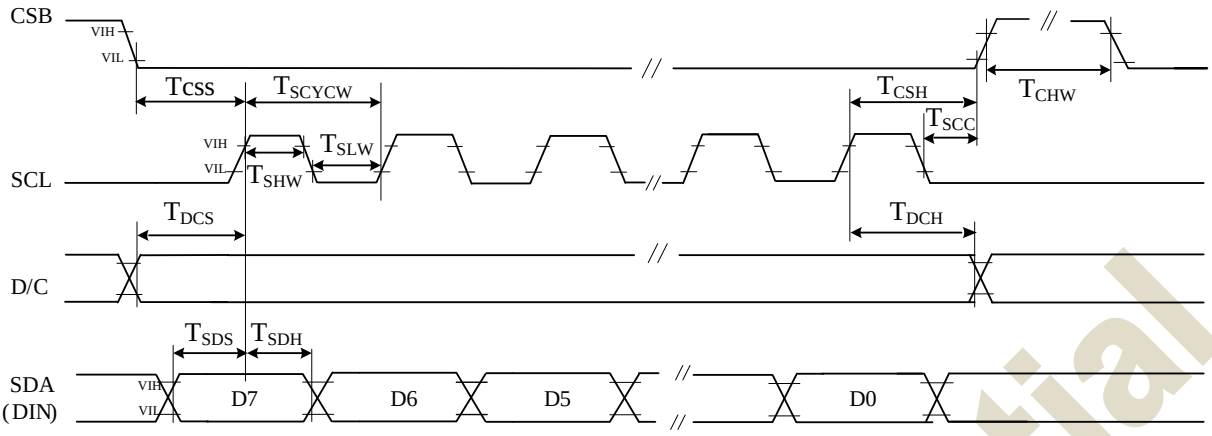
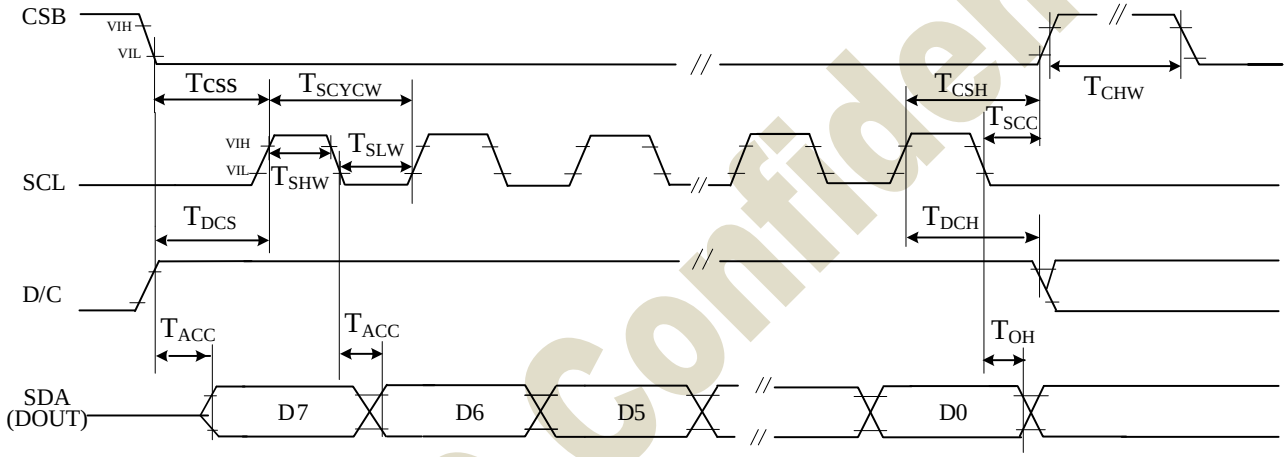
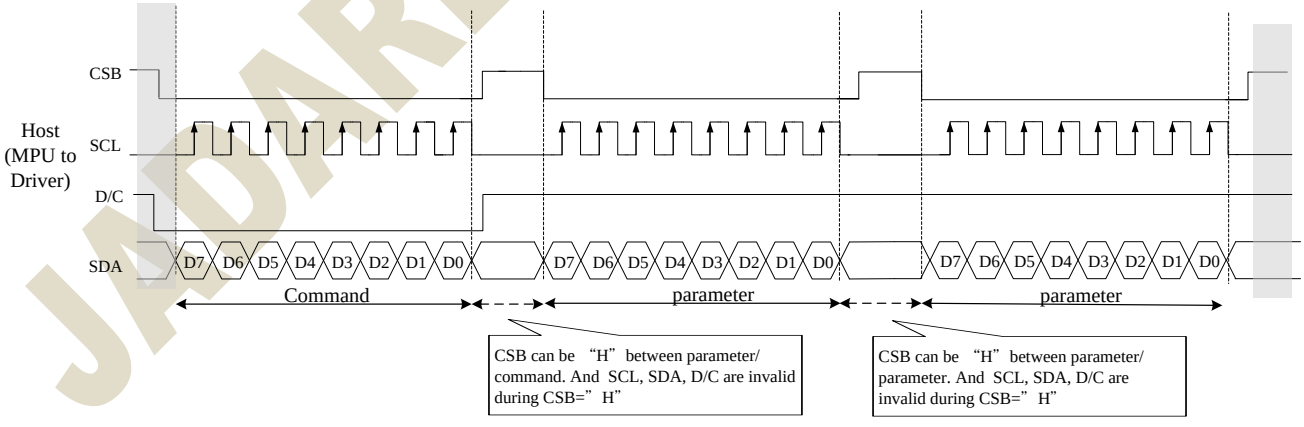
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



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8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79661AA. Refer to the next section for detail register function description.

Address	command			Bit								
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna	FR[2:0]			02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

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R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(8)	VRES(0)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	0	0	1	1	03h
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	-	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMOD	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
R9FH	Read MTP Reserved Bytes(RMRB)	W	0	1	0	0	1	1	1	1	1	9FH
		R	1	#	#	#	#	#	#	#	#	-
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h

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8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1 R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source/Boder/Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 176x296 (default) 01: Display resolution is 128x296 10: Display resolution is 128x250 11: Display resolution is 112x204

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2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display,the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

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8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

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3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

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5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

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Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	10v	+10v
	VGN	10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

4. Voltage setting limit: VSP_0 ≥ VSPL_0 , VSP_1 ≥ VSPL_1

Restriction	

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8.2.3R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R02h =0x00 ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

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8.2.4 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence(base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

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8.2.5 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

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Description

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		

Restriction

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8.2.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

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8.2.7 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM	W	0	0	0	0	1	0	0	0	0	10H
2 bit mode	W	1									
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
:	W	1	:		:		:		:		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel. Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction	

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8.2.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / Data_flag / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

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8.2.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DC VCOM	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12h=0x00 While users send this command, driver will refresh display base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

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8.2.10 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

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8.2.13 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

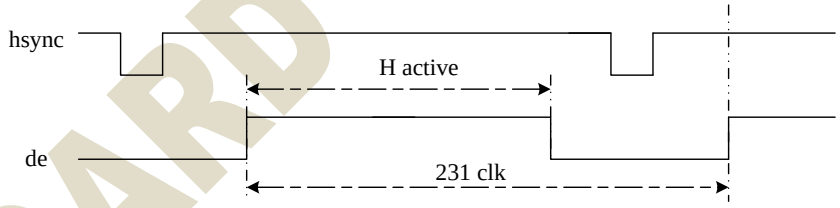
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

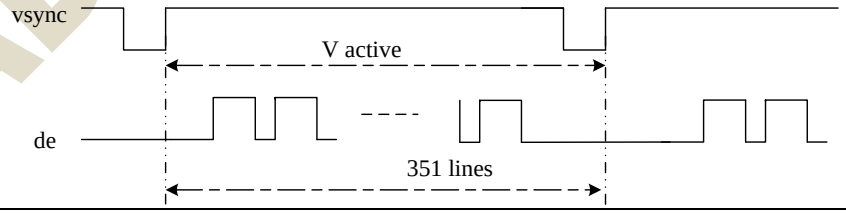
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

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8.2.14 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

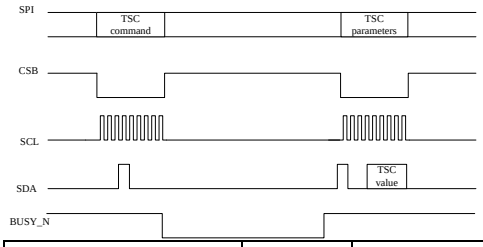
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

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8.2.15 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

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8.2.16 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction: This command only actives after R04H(PON)

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8.2.17 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

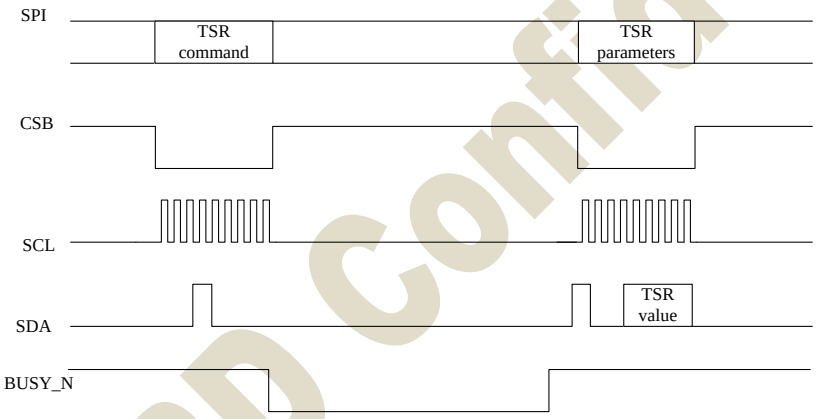
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON)

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8.2.18 R50H (CDI): VCOM and DATA interval setting Register

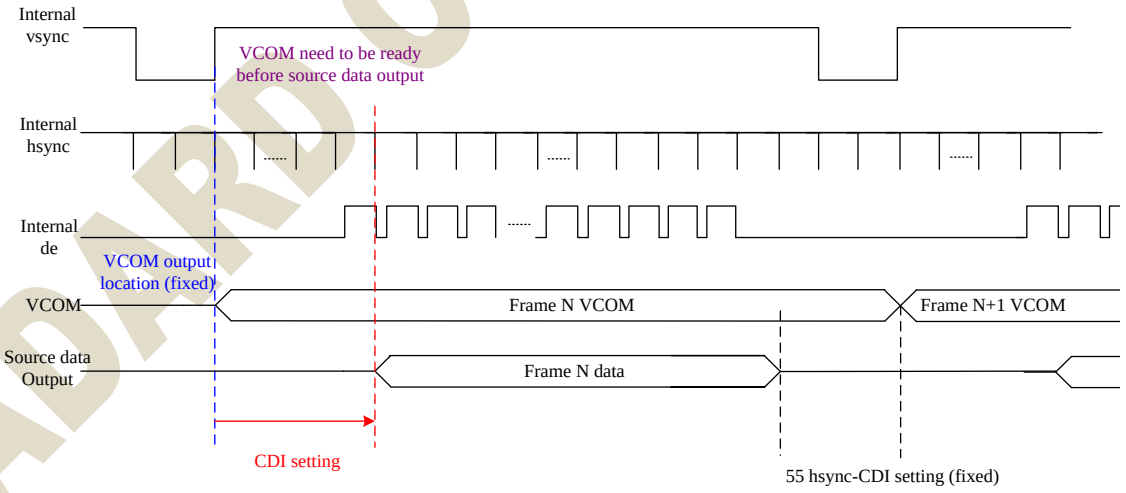
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



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VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

Boarder output will follow FOPT definition being defined in R00h.

Restriction	

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8.2.19 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

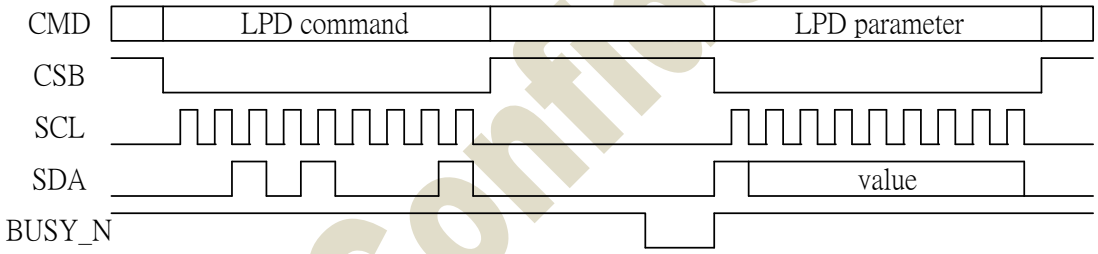
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status.



Restriction: This command only actives when BUSY_N = "1".

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8.2.20 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[9:8],HRES[1:0],VRST[9] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :176X296 GD: First G active = G0 LAST active GD= 0+296-1= 295; (G295) SD : First active channel: =S0 LAST active SD=0+44*4-1=175; (S175) Note : Only supports source 176.ch for source 160ch. above
Restriction	Horizontal resolution should be 4-multiple.

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8.2.21 R65H(GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Note: No matter S_start[9:8], S_start [1:0],VRST[9] value being filled, it's always be 00b. 1.S_Start [7:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line
Restriction	S_Start should be the multiple of 4

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8.2.22 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	0	0	1	1	03h
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

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8.2.23 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

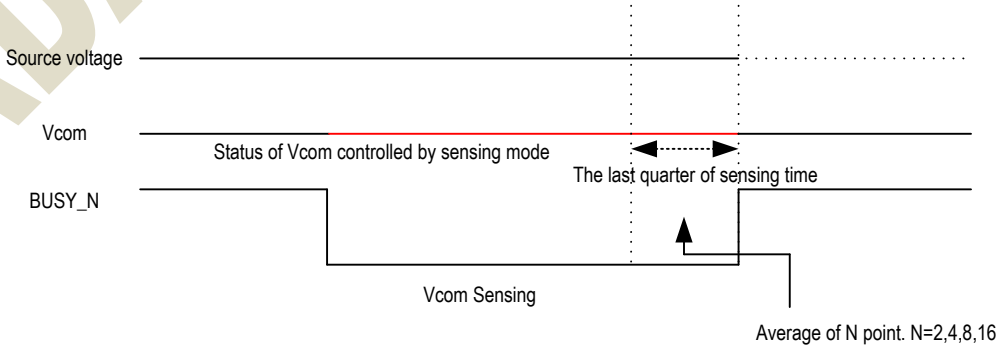
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction: This command only actives when BUSY_N = "1".

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8.2.24 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
6-0	VV[6:0]	**VCOM value**

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

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8.2.25 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Name	Description
6-0	VDCS[6:0]	VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

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	7	MTP_VCM	Follow MTP VCOM value in MTP mode 0: From the setting of MTP (default) 1:From the setting of register
Restriction			

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8.2.26 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	-	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode

Note:
No matter HRST[1:0] ,HRST[9:8],HRED[9:8],VRST[9],VRED[9] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Restriction

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8.2.27 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

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8.2.28 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

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8.2.29 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the MTP								-

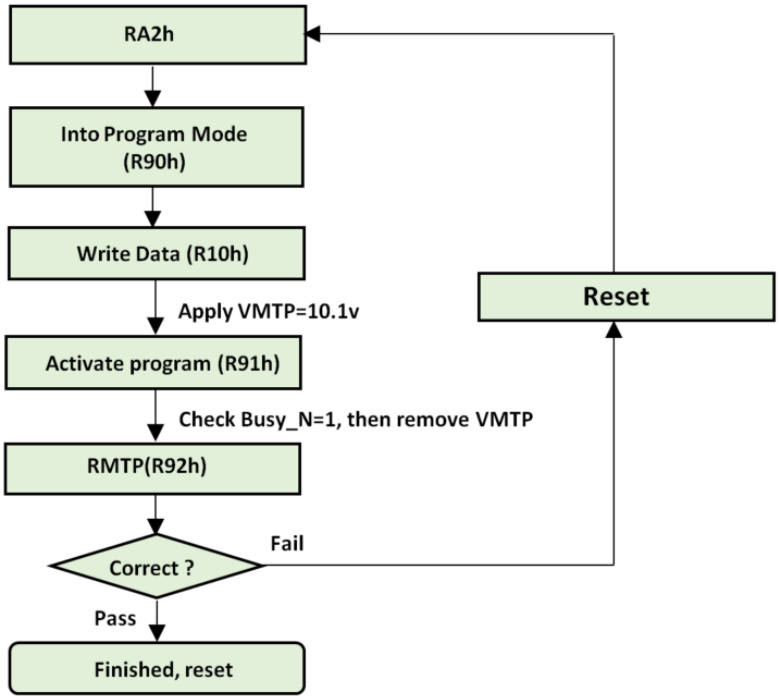
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

The command is used for reading the content of MTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF



The sequence of programming MTP(External power)

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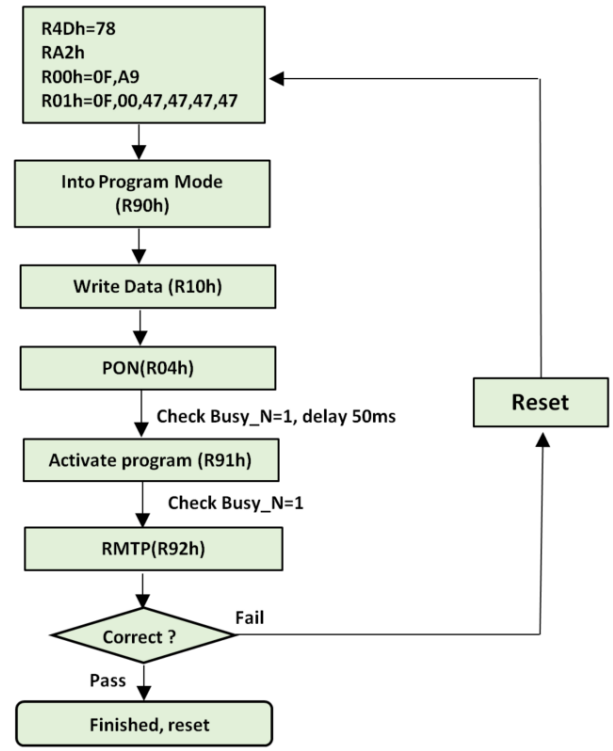

The sequence of programming MTP(Internal power)

Restriction	This command only actives when BUSY_N = “1”.

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8.2.30 R9FH(RMRB) Read MTP Reserved Bytes

R9FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMRB	W	0	1	0	0	1	1	1	1	1	9FH
1st Parameter	R	1	Dummy								00h
2nd Parameter	R	1	The data of address 0x16F7 in the MTP								00h
3rd Parameter	R	1	:								00h
:	R	1	:								00h
97th Parameter	R	1	:								00h
98th Parameter	R	1	:								00h
101th Parameter	R	1	The data of address 0x175A in the MTP								00h

Description	-The command define as follows: The command is used for reading the content of MTP Reserved Byte for checking the data of programming. This command could read these information from MTP directly.
Restriction	

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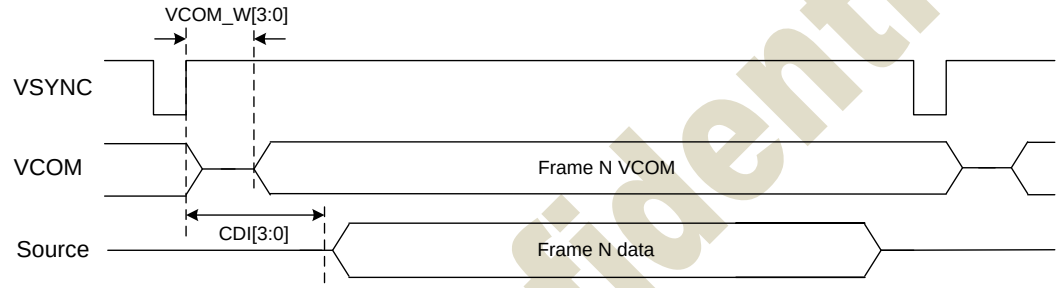
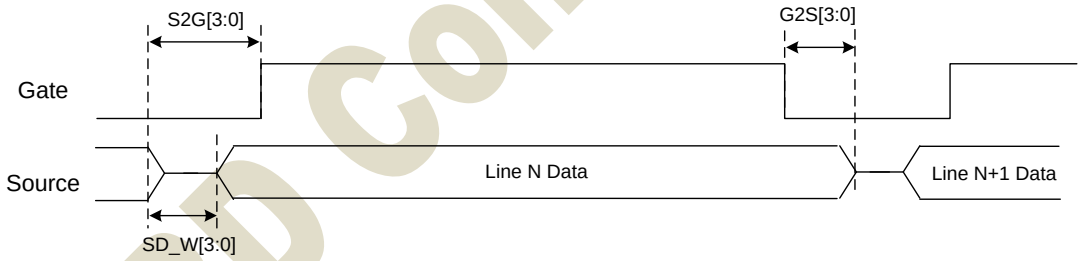
8.2.31 RE3H (PWS): Power Saving Register

RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. VCOM_W: VCOM power saving width (unit = line period)  SD_W: Source power saving width (unit = 500nS), SD_W<=S2G 
Restriction	

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8.2.32 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

Restriction	

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Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R04H(PON)	X	Flag
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R17H(AUTO)	Valid in standby	Flag
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R61H(TRES)	X	No action
R65H(GSST)	X	No action
R70H(REV)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R83H(PTL)	X	No action
R90H(PGM)	X	No action
R91H(APG)	X	Flag
R92H(RMTP)	X	Flag
R9FH(Read MTP reserved)	Valid only read	Flag
RE3H(PWS)	X	No action
RE4H(LVSEL)	X	No action

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9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

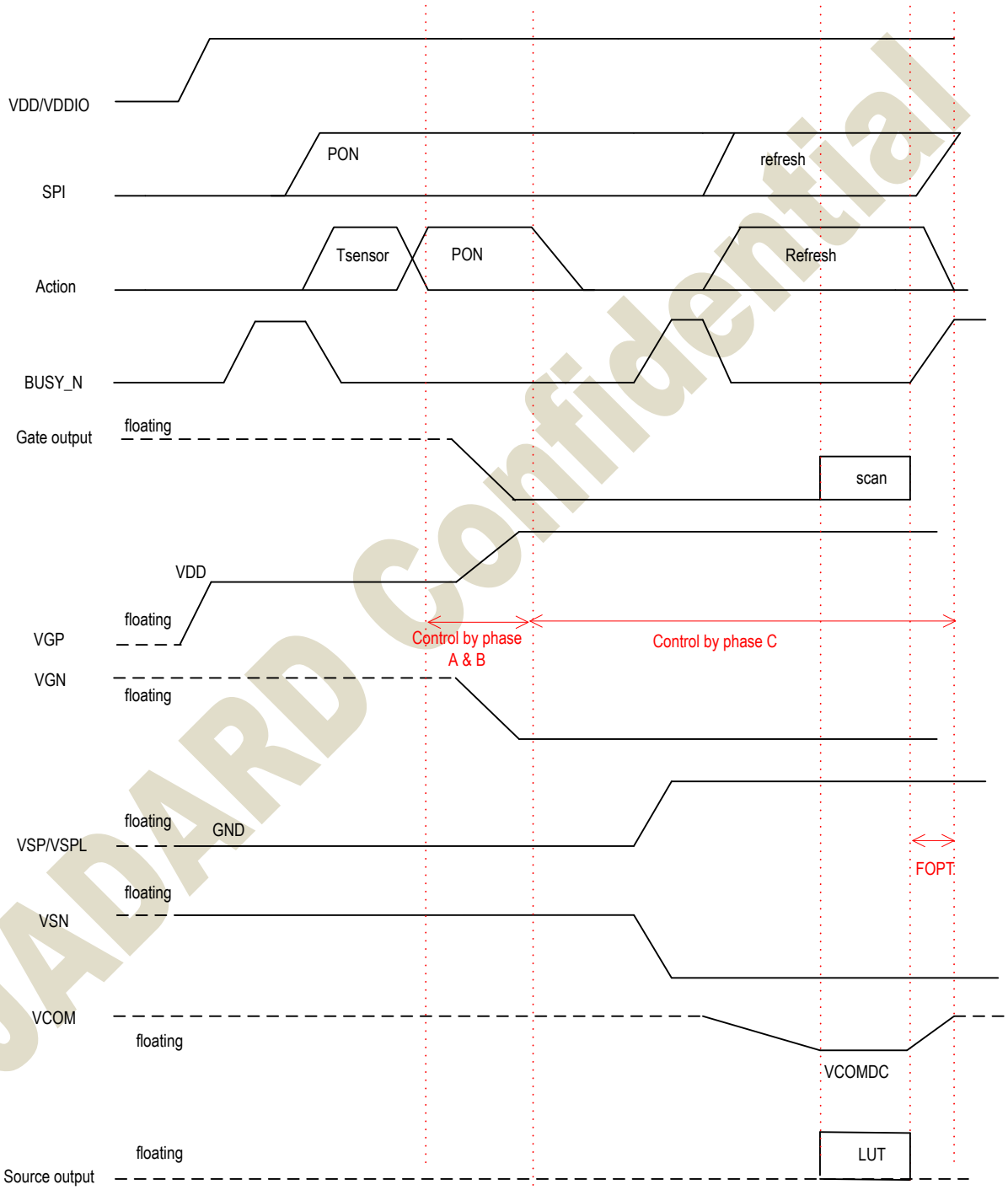

Figure 1: Power on sequence

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Power off Sequence

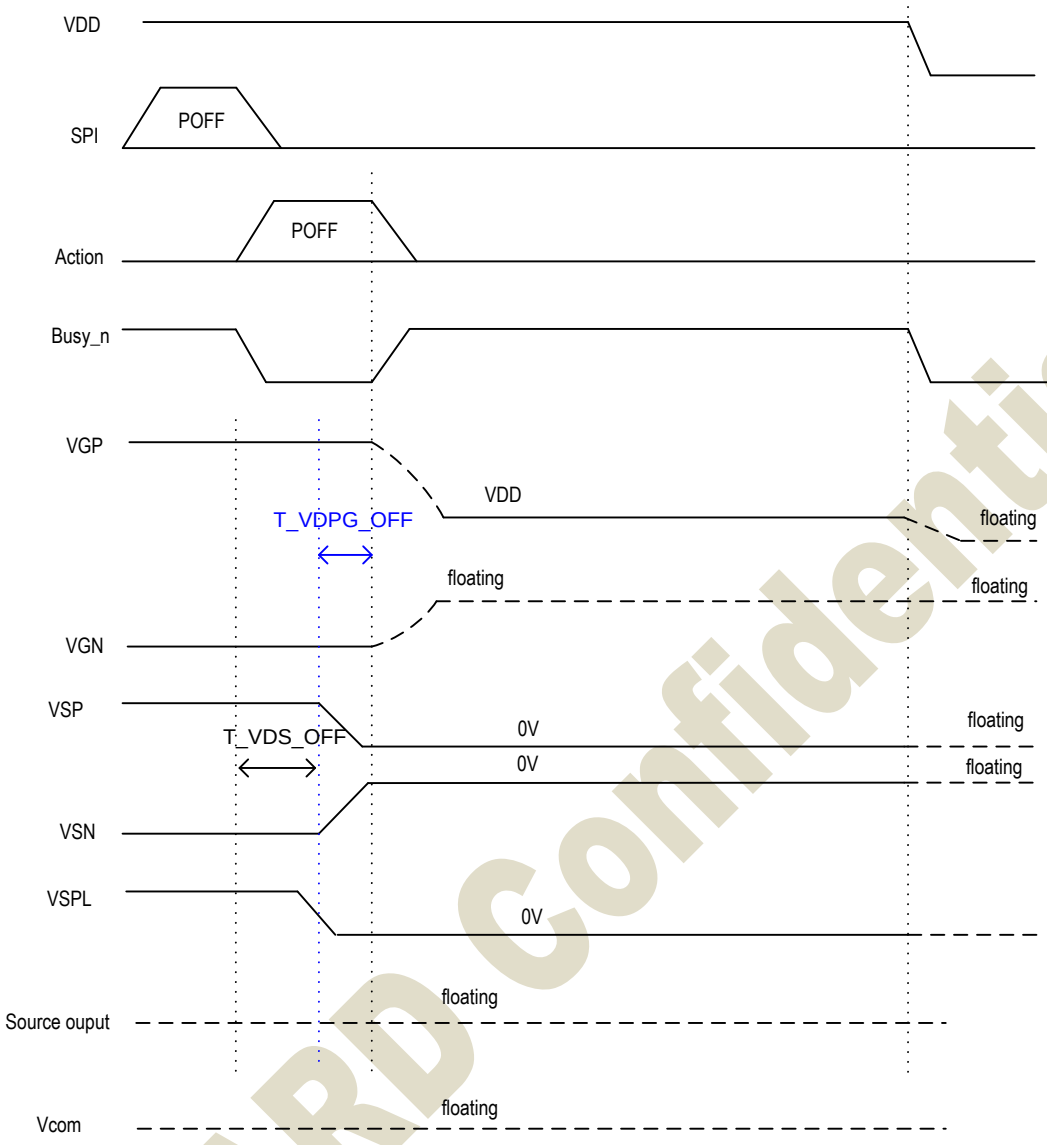

Figure 2: Power off sequence

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DSLP sequence

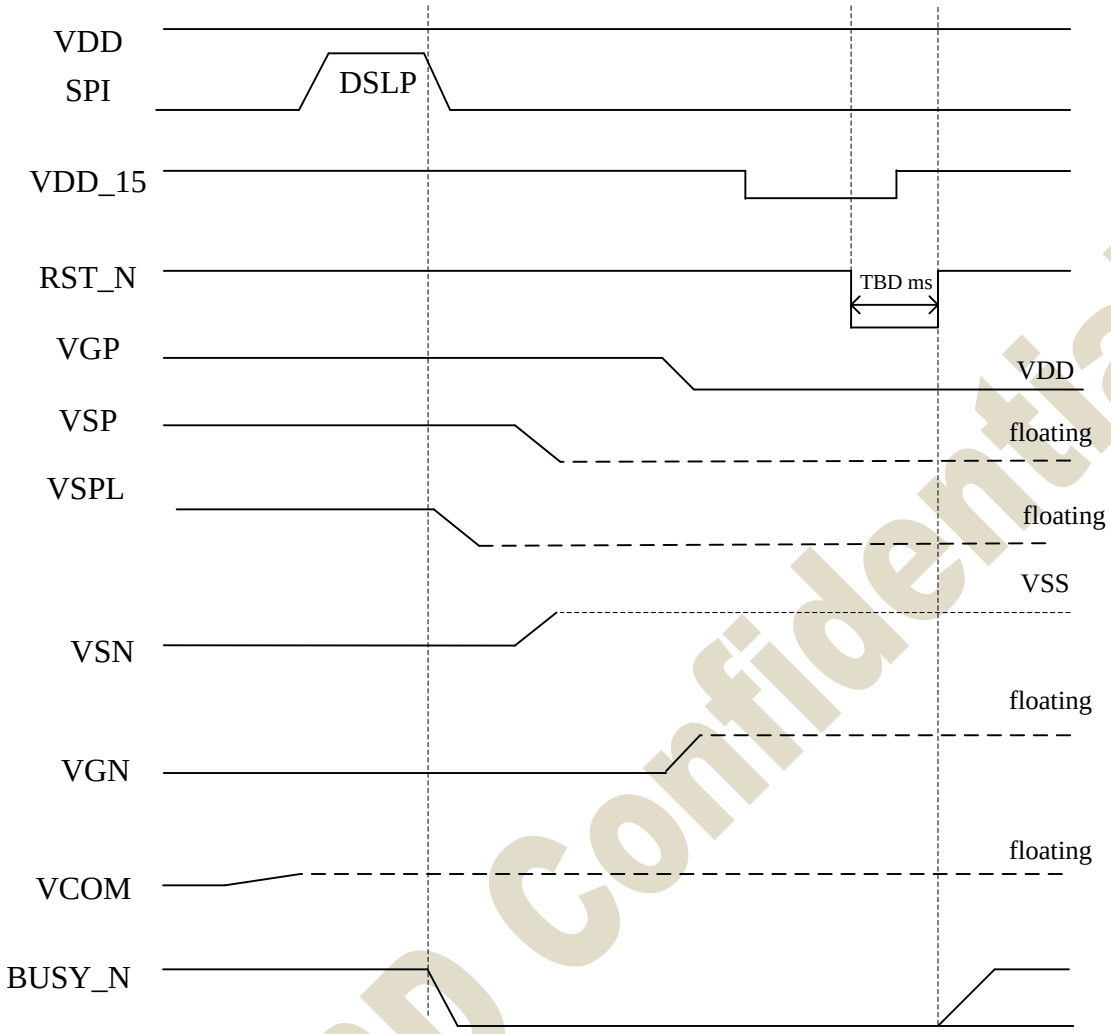

Figure 3: DSLP sequence

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9.2 MTP LUT Definition

The MTP size would be 6144 Bytes.

MTP bank 0 (6K bytes)	
Address(Hex)	Content
0x0000~0x15DF	LUT Compress data
0x15E0~0x16F6	Reserved bytes
0x16F7~0X175A	User Reserved bytes(R9FH)
0x175B~0x1784	Default setting
0x1785~0x17FF	JD setting

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Default Setting Format in MTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
R9FH	5879-5978	16F7-175A	User Reserved bytes								FF
--	5979	175B	Enable MTP Setting (0xA5)								A5
R00H	5980	175C	RES[1:0]		PST_MODE	-	UD	SHL	SHD_N	RST_N	0F
	5981	176D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09
R01H	5982	175E	-	-	-	-	V_MODE	VSC_EN	VDS_EN	VDG_EN	07
	5983	175F	-	-	-		-	-	VGP[1:0]		00
	5984	1760	-	VSPL_0[6:0]							00
	5985	1761	-	VSP_1[6:0]							00
	5986	1762	-	VSN_1[6:0]							00
	5987	1763	-	VSPL_1[6:0]							00
-	5988	1764	Reserved								00
	5989	1765	Reserved								00
	5990	1766	Reserved								54
	5991	1767	Reserved								44
R06H	5992	1768	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00
	5993	1769	-	-	PHA_ON[5:0]						06
	5994	176A	-	-	PHA_OFF[5:0]						02
	5995	176B	-	-	PHB_ON[5:0]						07
	5996	176C	-	-	PHB_OFF[5:0]						02
	5997	176D	-	-	PHC_ON[5:0]						07
	5998	176E	-	-	PHC_OFF[5:0]						02
-	5999	177F	Reserved								00
R30H	6000	1770	-	-	-	-	Dyna	FR[2:0]			02
R50h	6001	1771	VBD[2:0]			DDX	CDI[3:0]				97
R60H	6002	1772	-	-	S2G[5:0]						02
	6003	1773	-	-	G2S[5:0]						02
R61H	6004	1774	-	-	-	-	-	-	HRES[9]	HRES[8]	00
	6005	1775	HRES[7:3]						0	0	00
	6006	1776	-	-	-	-	-	-	VRES[9]	VRES[8]	00
	6007	1777	VRES[7:0]								00
R65H	6008	1778	-	-	-	-	-	-	S_start(9)	S_start(8)	00
	6009	1779	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00
	6010	177A	-	-	-	-	-	-	G_start(9)	G_start(8)	00
	6011	177B	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00
-	6012	177C	Reserved								FF
	6013	177D	Reserved								FF
	6014	177E	Reserved								FF
	6015	177F	Reserved								00
RE3H	6016	1780	VCOM_W[3:0]				SD_W[3:0]				00
RE4H	6017	1781	-	-	-	-	-	-	LVD_SEL[1:0]		03
-	6018	1782	Reserved								03
	6019	1783	Reserved								1C
	6020	1784	Reserved								00
--	6021-6143	1785-17FF	JD setting								FF

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9.3 Data transmission waveform

Example1: The driver will scan 1 frame to GND after waveform finished.(FOPT=0)

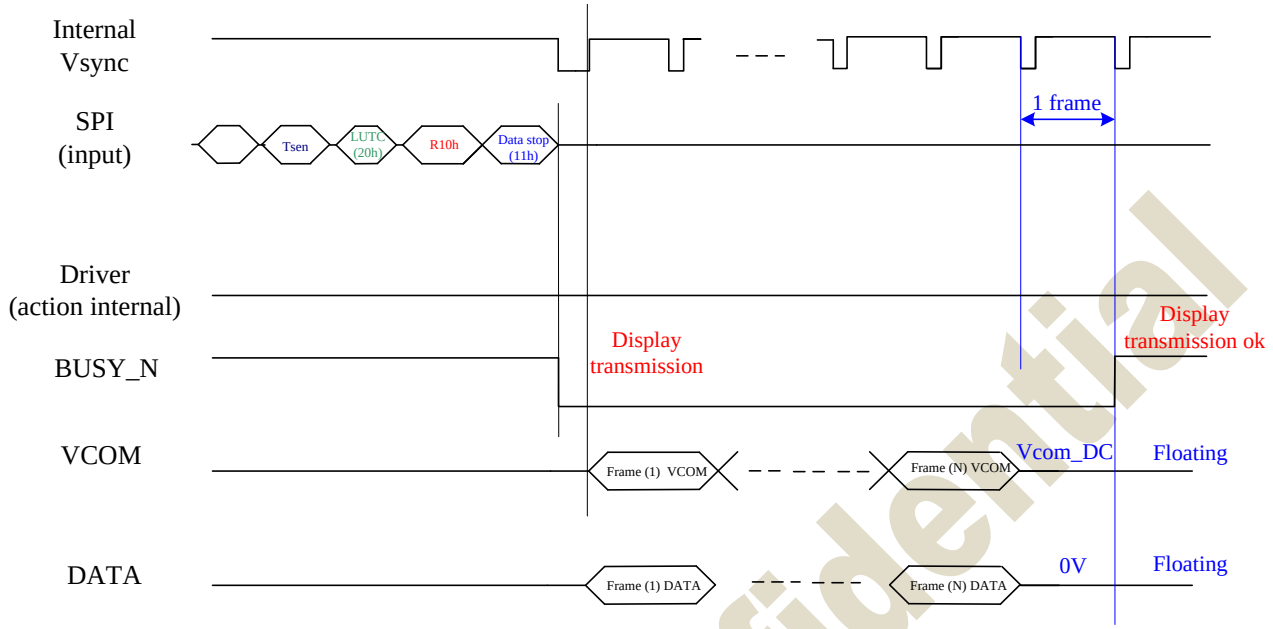

Figure 1: Data transmission example1 waveform

Example2: The driver will float VCOM and keep previous output data(FOPT=1)

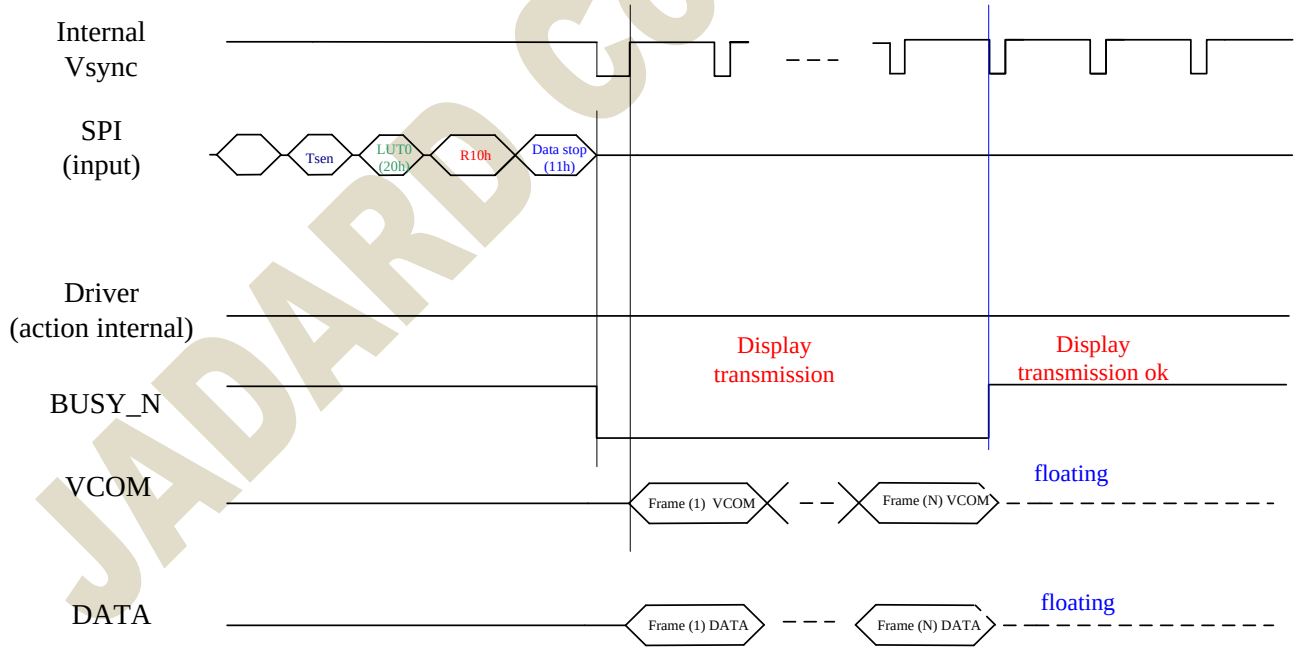

Figure 2: Display refresh example2 waveform

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10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGP-VGN	VGN-0.3	VGP+0.3	V
Analog supply	VSP_0	+15	+15	V
Analog supply	VSN_0	-15	-15	V
Analog supply	VSPL_0	+3	+15	V
Analog supply	VSP_1	+3	+15	V
Analog supply	VSN_1	-3	-15	V
Analog supply	VSPL_1	+3	+15	V
Supply voltage	VGP	+10	+20	V
Supply voltage	VGN	-20	-10	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

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10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
MTP program power	VMTP	9.8	10.1	10.2		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3Xvdd	V	Digital input pins
High Level Input Voltage	Vih	0.7Xvio	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400uA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400uA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL= -400 uA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	mA	No load
Operating Current	IVDD1*	-	-	TBD	mA	
Operating temperature	T_{op}	-30	-	85	℃	

NOTE: typ. and max. values to be confirmed by design

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10.3 Analog DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSP	-	15	-	V	For source driver/VCOM
Positive Source voltage dev	dvsp	-100	0	+100	mV	
Negative Source voltage	VSn	-	-15	-	V	For source driver/VCOM
Negative Source voltage dev	dvsn	-100	-	+100	mV	
Positive Source voltage	VSPL_0	3		15	V	
Positive Source voltage dev.	dvspl_0	-100	-	+100	mV	
Positive Source voltage	VSP_1	3		15	V	
Positive Source voltage dev.	dvsp_1	-100	-	+100	mV	
Positive Source voltage	VSPL_1	3		15	V	
Positive Source voltage dev.	dvspl_1	-100	-	+100	mV	
VCOM voltage dev.	dvcom	-200	-	+200	mV	
Positive gate voltage dev	dvgp	-500	-	+500	mV	
Dynamic Range of Output	Vdr	0.1	-	VSP-0.1	V	
Voltage Range of VGP – VGN	VGP-VGN	-	-	41	V	
Negative Gate voltage	VGN	-10	-	-20	V	For gate driver
Positive Gate voltage	VGP	10		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGP*	-	0	0.2	uA	Include VSP power With load
Positive HV Operating Current	IVGP*	-	0.7	1.1	mA	Include VSP power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGP*	-	0.8	1.2	mA	Include VSP power With load all SD=H VCOM external resistor divider not Included
Negative HV Stand-by Current (power off mode)	IstVGN*	-	0	0.2	uA	Include VSP power With load
Negative HV Operating Current	IVGN*	-	0.8	1.2	mA	Include VSN power With load all SD=L
Negative HV Operating Current	IVGN*	-	0.9-	1.3	mA	Include VSN power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*	-	0	0.01	uA	
VINT1 Operating Current	IVINT1*	-	-	0.3	mA	
Voltage	IVINT1*	-	-	0.3	mA	

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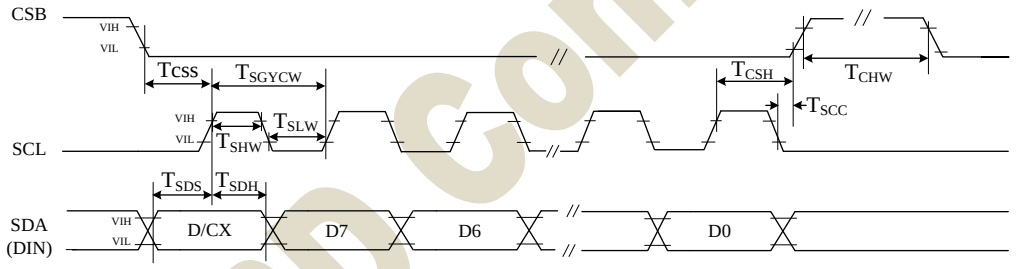
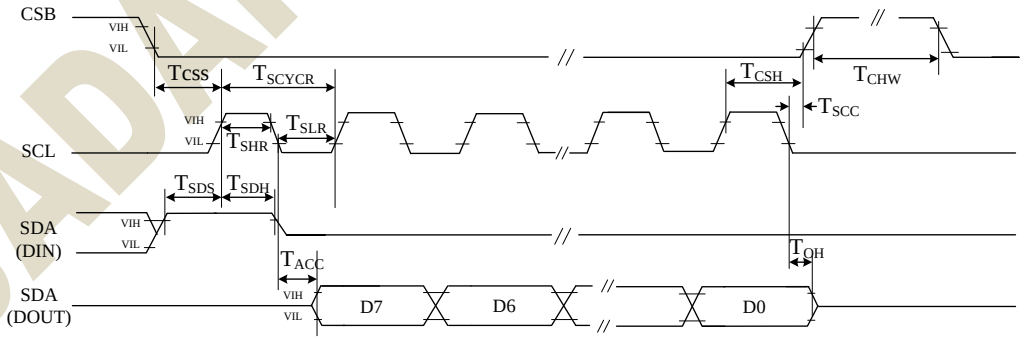
10.4 AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	150			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			10	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)

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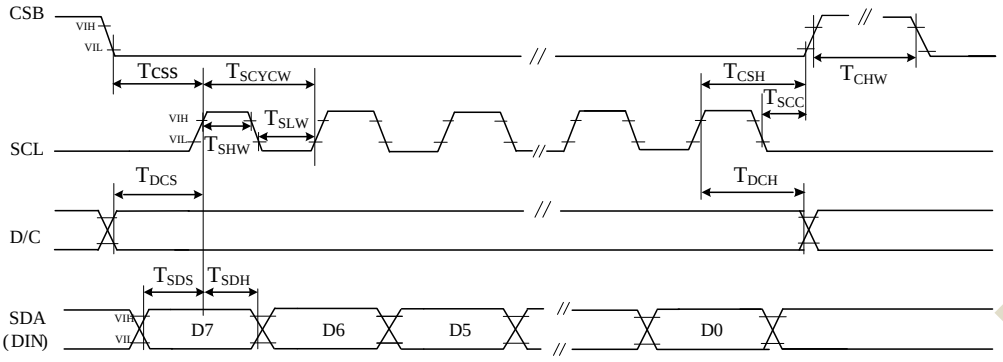
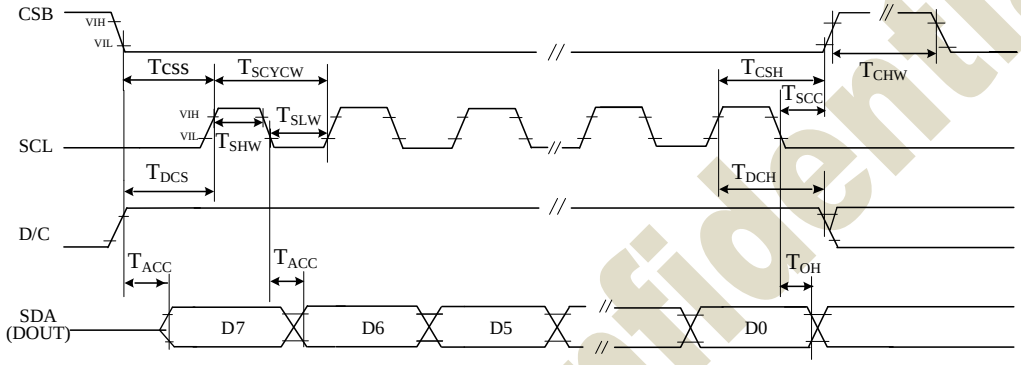


4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 9: SPI interface timing

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11. CHIP OUTLINE DIMENSIONS

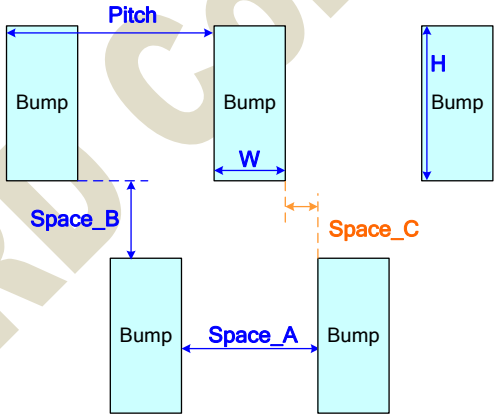
11.1 Circuit/Bump View

G1 G3 G5 ... S_ADDE7~S_ADDE0 S159~S0 S_ADDS7~S_ADDS0 ... G4 G2 G0

JD79661AA
(face up)

Die Size:	9531um*981um (include scribe line 60um)
Die Thickness:	230 μm ± 20μm (Polish)
Die TTV:	$(D_{MAX} – D_{MIN})$ within die ≤ 2μm
Bump Height:	9 μm ± 2μm
	$(H_{MAX} – H_{MIN})$ within die ≤ 2μm
Hardness:	75 Hv ±25Hv
Coordinate origin:	Chip center

11.2 Bump information



Bump type	Pitch	Space_A	Space_B	Space_C	W	H	Area(um2)	Q'ty	Total area(um2)
Input PAD	46	18	-	-	28	70	1960	203	397880
Source PAD	26	14	19	1	12	100	1200	180	216000
Gate PAD	42	24	25	3	18	75	1350	312	421200
							Total	695	1035080

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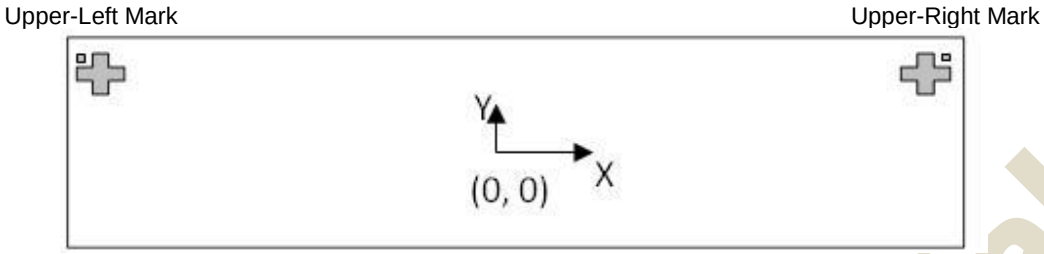
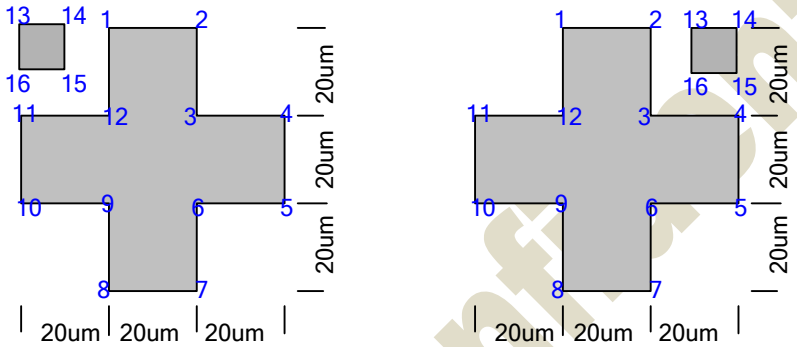
12. ALIGNMENT MARK INFORMATION

12.1 Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-4665	390	4665	390
1	-4675	420	4655	420
2	-4655	420	4675	420
3	-4655	400	4675	400
4	-4635	400	4695	400
5	-4635	380	4695	380
6	-4655	380	4675	380
7	-4655	360	4675	360
8	-4675	360	4655	360
9	-4675	380	4655	380
10	-4695	380	4635	380
11	-4695	400	4635	400
12	-4675	400	4655	400
13	-4695	420	4685	420
14	-4685	420	4695	420
15	-4685	410	4695	410
16	-4695	410	4685	410

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12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	DUMMY	-4646	-398	28	70
2	VCOM	-4600	-398	28	70
3	VCOM	-4554	-398	28	70
4	VCOM	-4508	-398	28	70
5	VCOM	-4462	-398	28	70
6	VCOM	-4416	-398	28	70
7	VCOM	-4370	-398	28	70
8	VCOM	-4324	-398	28	70
9	VCOM	-4278	-398	28	70
10	VSSA	-4232	-398	28	70
11	VGL	-4186	-398	28	70
12	VGL	-4140	-398	28	70
13	VGL	-4094	-398	28	70
14	VGL	-4048	-398	28	70
15	VGL	-4002	-398	28	70
16	VGL	-3956	-398	28	70
17	VGL	-3910	-398	28	70
18	VGL	-3864	-398	28	70
19	VGL	-3818	-398	28	70
20	VGL	-3772	-398	28	70
21	VGL	-3726	-398	28	70
22	VGL	-3680	-398	28	70
23	VGL	-3634	-398	28	70
24	VGL	-3588	-398	28	70
25	VGL	-3542	-398	28	70
26	VGL	-3496	-398	28	70
27	VSSA	-3450	-398	28	70
28	VSL	-3404	-398	28	70
29	VSL	-3358	-398	28	70
30	VSL	-3312	-398	28	70
31	VSL	-3266	-398	28	70
32	VSL	-3220	-398	28	70
33	VSL	-3174	-398	28	70
34	VSL	-3128	-398	28	70
35	VSL	-3082	-398	28	70
36	VSL	-3036	-398	28	70
37	VSL	-2990	-398	28	70
38	VSSA	-2944	-398	28	70
39	VGH	-2898	-398	28	70
40	VGH	-2852	-398	28	70
41	VGH	-2806	-398	28	70
42	VGH	-2760	-398	28	70
43	VGH	-2714	-398	28	70
44	VGH	-2668	-398	28	70
45	VGH	-2622	-398	28	70
46	VGH	-2576	-398	28	70
47	VGH	-2530	-398	28	70
48	VGH	-2484	-398	28	70
49	VGH	-2438	-398	28	70
50	VGH	-2392	-398	28	70
51	VSSA	-2346	-398	28	70
52	VSH	-2300	-398	28	70
53	VSH	-2254	-398	28	70
54	VSH	-2208	-398	28	70
55	VSH	-2162	-398	28	70
56	VSH	-2116	-398	28	70
57	VSH	-2070	-398	28	70
58	VSH	-2024	-398	28	70

No.	Name	X-axis	Y-axis	W	H
59	VSH	-1978	-398	28	70
60	VSH	-1932	-398	28	70
61	VSH	-1886	-398	28	70
62	VSSA	-1840	-398	28	70
63	VOTP	-1794	-398	28	70
64	VOTP	-1748	-398	28	70
65	VOTP	-1702	-398	28	70
66	VOTP	-1656	-398	28	70
67	VOTP	-1610	-398	28	70
68	VOTP	-1564	-398	28	70
69	VDD_18V	-1518	-398	28	70
70	VDD_18V	-1472	-398	28	70
71	VDD_18V	-1426	-398	28	70
72	VDD_18V	-1380	-398	28	70
73	VDD_18V	-1334	-398	28	70
74	VDD_18V	-1288	-398	28	70
75	VDD_18V	-1242	-398	28	70
76	VDD_18V	-1196	-398	28	70
77	VSSA	-1150	-398	28	70
78	VSSA	-1104	-398	28	70
79	VSSA	-1058	-398	28	70
80	VSSA	-1012	-398	28	70
81	VSSA	-966	-398	28	70
82	VSSA	-920	-398	28	70
83	VSSA	-874	-398	28	70
84	VSSA	-828	-398	28	70
85	VSSA	-782	-398	28	70
86	VSSA	-736	-398	28	70
87	VSSA	-690	-398	28	70
88	VSSA	-644	-398	28	70
89	VSS	-598	-398	28	70
90	VSS	-552	-398	28	70
91	VSS	-506	-398	28	70
92	VSS	-460	-398	28	70
93	VSS	-414	-398	28	70
94	VSS	-368	-398	28	70
95	VSS	-322	-398	28	70
96	VSS	-276	-398	28	70
97	VSS	-230	-398	28	70
98	VSS	-184	-398	28	70
99	T_IN[1]	-138	-398	28	70
100	T_IN[0]	-92	-398	28	70
101	VDD	-46	-398	28	70
102	VDD	0	-398	28	70
103	VDD	46	-398	28	70
104	VDD	92	-398	28	70
105	VDD	138	-398	28	70
106	VDD	184	-398	28	70
107	VDD	230	-398	28	70
108	VDD	276	-398	28	70
109	VDD	322	-398	28	70
110	VDD	368	-398	28	70
111	VDDIO	414	-398	28	70
112	VDDIO	460	-398	28	70
113	VDDIO	506	-398	28	70
114	VDDIO	552	-398	28	70
115	VDDIO	598	-398	28	70
116	VDDIO	644	-398	28	70

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No.	Name	X-axis	Y-axis	W	H
117	VDDIO	690	-398	28	70
118	T_DEBUG[7]	736	-398	28	70
119	T_DEBUG[6]	782	-398	28	70
120	VDDP	828	-398	28	70
121	VDDP	874	-398	28	70
122	VDDP	920	-398	28	70
123	VDDP	966	-398	28	70
124	T_DEBUG[5]	1012	-398	28	70
125	T_DEBUG[4]	1058	-398	28	70
126	T_DEBUG[4]	1104	-398	28	70
127	T_DEBUG[3]	1150	-398	28	70
128	T_DEBUG[3]	1196	-398	28	70
129	DUMMY[1]	1242	-398	28	70
130	SDA	1288	-398	28	70
131	SCL	1334	-398	28	70
132	VSS	1380	-398	28	70
133	CSB	1426	-398	28	70
134	VDDIO	1472	-398	28	70
135	T_DEBUG[2]	1518	-398	28	70
136	VSS	1564	-398	28	70
137	DC	1610	-398	28	70
138	VDDIO	1656	-398	28	70
139	T_DEBUG[1]	1702	-398	28	70
140	VSS	1748	-398	28	70
141	RST_N	1794	-398	28	70
142	BUSY_N	1840	-398	28	70
143	SYNCC	1886	-398	28	70
144	VDDIO	1932	-398	28	70
145	T_DEBUG[8]	1978	-398	28	70
146	VSS	2024	-398	28	70
147	T_DEBUG[0]	2070	-398	28	70
148	VDDIO	2116	-398	28	70
149	BS	2162	-398	28	70
150	VSS	2208	-398	28	70
151	T_EN_DIG	2254	-398	28	70
152	VDDIO	2300	-398	28	70
153	PCKI	2346	-398	28	70
154	VSS	2392	-398	28	70
155	MS	2438	-398	28	70
156	VDDIO	2484	-398	28	70
157	TSDA	2530	-398	28	70
158	TSDA	2576	-398	28	70
159	TSCL	2622	-398	28	70
160	TSCL	2668	-398	28	70
161	PCKO	2714	-398	28	70
162	SYNCD	2760	-398	28	70
163	T_EX_SYSCLK	2806	-398	28	70
164	T_EX_REFCLK	2852	-398	28	70
165	VSHR	2898	-398	28	70
166	VSHR	2944	-398	28	70
167	VSHR	2990	-398	28	70
168	VSHR	3036	-398	28	70
169	VSHR	3082	-398	28	70
170	VSHR	3128	-398	28	70
171	VSHR	3174	-398	28	70
172	VSHR	3220	-398	28	70
173	DUMMY[2]	3266	-398	28	70
174	DUMMY[3]	3312	-398	28	70
175	DUMMY[4]	3358	-398	28	70
176	DUMMY[5]	3404	-398	28	70

No.	Name	X-axis	Y-axis	W	H
177	DUMMY[6]	3450	-398	28	70
178	DUMMY[7]	3496	-398	28	70
179	VSSA	3542	-398	28	70
180	FB	3588	-398	28	70
181	FB	3634	-398	28	70
182	VSSA	3680	-398	28	70
183	RESE	3726	-398	28	70
184	RESE	3772	-398	28	70
185	VSSA	3818	-398	28	70
186	GDR	3864	-398	28	70
187	GDR	3910	-398	28	70
188	GDR	3956	-398	28	70
189	GDR	4002	-398	28	70
190	GDR	4048	-398	28	70
191	GDR	4094	-398	28	70
192	GDR	4140	-398	28	70
193	GDR	4186	-398	28	70
194	VSSA	4232	-398	28	70
195	VCOM	4278	-398	28	70
196	VCOM	4324	-398	28	70
197	VCOM	4370	-398	28	70
198	VCOM	4416	-398	28	70
199	VCOM	4462	-398	28	70
200	VCOM	4508	-398	28	70
201	VCOM	4554	-398	28	70
202	VCOM	4600	-398	28	70
203	DUMMY[8]	4646	-398	28	70
204	T_EN_LSH	4540	313.5	18	75
205	T_VREF	4519	413.5	18	75
206	T_VTSEN	4498	313.5	18	75
207	T_IBIAS	4477	413.5	18	75
208	T_SAR_REF	4456	313.5	18	75
209	DUMMY[9]	4435	413.5	18	75
210	G[0]	4414	313.5	18	75
211	G[2]	4393	413.5	18	75
212	G[4]	4372	313.5	18	75
213	G[6]	4351	413.5	18	75
214	G[8]	4330	313.5	18	75
215	G[10]	4309	413.5	18	75
216	G[12]	4288	313.5	18	75
217	G[14]	4267	413.5	18	75
218	G[16]	4246	313.5	18	75
219	G[18]	4225	413.5	18	75
220	G[20]	4204	313.5	18	75
221	G[22]	4183	413.5	18	75
222	G[24]	4162	313.5	18	75
223	G[26]	4141	413.5	18	75
224	G[28]	4120	313.5	18	75
225	G[30]	4099	413.5	18	75
226	G[32]	4078	313.5	18	75
227	G[34]	4057	413.5	18	75
228	G[36]	4036	313.5	18	75
229	G[38]	4015	413.5	18	75
230	G[40]	3994	313.5	18	75
231	G[42]	3973	413.5	18	75
232	G[44]	3952	313.5	18	75
233	G[46]	3931	413.5	18	75
234	G[48]	3910	313.5	18	75
235	G[50]	3889	413.5	18	75
236	G[52]	3868	313.5	18	75

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No.	Name	X-axis	Y-axis	W	H
237	G[54]	3847	413.5	18	75
238	G[56]	3826	313.5	18	75
239	G[58]	3805	413.5	18	75
240	G[60]	3784	313.5	18	75
241	G[62]	3763	413.5	18	75
242	G[64]	3742	313.5	18	75
243	G[66]	3721	413.5	18	75
244	G[68]	3700	313.5	18	75
245	G[70]	3679	413.5	18	75
246	G[72]	3658	313.5	18	75
247	G[74]	3637	413.5	18	75
248	G[76]	3616	313.5	18	75
249	G[78]	3595	413.5	18	75
250	G[80]	3574	313.5	18	75
251	G[82]	3553	413.5	18	75
252	G[84]	3532	313.5	18	75
253	G[86]	3511	413.5	18	75
254	G[88]	3490	313.5	18	75
255	G[90]	3469	413.5	18	75
256	G[92]	3448	313.5	18	75
257	G[94]	3427	413.5	18	75
258	G[96]	3406	313.5	18	75
259	G[98]	3385	413.5	18	75
260	G[100]	3364	313.5	18	75
261	G[102]	3343	413.5	18	75
262	G[104]	3322	313.5	18	75
263	G[106]	3301	413.5	18	75
264	G[108]	3280	313.5	18	75
265	G[110]	3259	413.5	18	75
266	G[112]	3238	313.5	18	75
267	G[114]	3217	413.5	18	75
268	G[116]	3196	313.5	18	75
269	G[118]	3175	413.5	18	75
270	G[120]	3154	313.5	18	75
271	G[122]	3133	413.5	18	75
272	G[124]	3112	313.5	18	75
273	G[126]	3091	413.5	18	75
274	G[128]	3070	313.5	18	75
275	G[130]	3049	413.5	18	75
276	G[132]	3028	313.5	18	75
277	G[134]	3007	413.5	18	75
278	G[136]	2986	313.5	18	75
279	G[138]	2965	413.5	18	75
280	G[140]	2944	313.5	18	75
281	G[142]	2923	413.5	18	75
282	G[144]	2902	313.5	18	75
283	G[146]	2881	413.5	18	75
284	G[148]	2860	313.5	18	75
285	G[150]	2839	413.5	18	75
286	G[152]	2818	313.5	18	75
287	G[154]	2797	413.5	18	75
288	G[156]	2776	313.5	18	75
289	G[158]	2755	413.5	18	75
290	G[160]	2734	313.5	18	75
291	G[162]	2713	413.5	18	75
292	G[164]	2692	313.5	18	75
293	G[166]	2671	413.5	18	75
294	G[168]	2650	313.5	18	75
295	G[170]	2629	413.5	18	75
296	G[172]	2608	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
297	G[174]	2587	413.5	18	75
298	G[176]	2566	313.5	18	75
299	G[178]	2545	413.5	18	75
300	G[180]	2524	313.5	18	75
301	G[182]	2503	413.5	18	75
302	G[184]	2482	313.5	18	75
303	G[186]	2461	413.5	18	75
304	G[188]	2440	313.5	18	75
305	G[190]	2419	413.5	18	75
306	G[192]	2398	313.5	18	75
307	G[194]	2377	413.5	18	75
308	G[196]	2356	313.5	18	75
309	G[198]	2335	413.5	18	75
310	G[200]	2314	313.5	18	75
311	G[202]	2293	413.5	18	75
312	G[204]	2272	313.5	18	75
313	G[206]	2251	413.5	18	75
314	G[208]	2230	313.5	18	75
315	G[210]	2209	413.5	18	75
316	G[212]	2188	313.5	18	75
317	G[214]	2167	413.5	18	75
318	G[216]	2146	313.5	18	75
319	G[218]	2125	413.5	18	75
320	G[220]	2104	313.5	18	75
321	G[222]	2083	413.5	18	75
322	G[224]	2062	313.5	18	75
323	G[226]	2041	413.5	18	75
324	G[228]	2020	313.5	18	75
325	G[230]	1999	413.5	18	75
326	G[232]	1978	313.5	18	75
327	G[234]	1957	413.5	18	75
328	G[236]	1936	313.5	18	75
329	G[238]	1915	413.5	18	75
330	G[240]	1894	313.5	18	75
331	G[242]	1873	413.5	18	75
332	G[244]	1852	313.5	18	75
333	G[246]	1831	413.5	18	75
334	G[248]	1810	313.5	18	75
335	G[250]	1789	413.5	18	75
336	G[252]	1768	313.5	18	75
337	G[254]	1747	413.5	18	75
338	G[256]	1726	313.5	18	75
339	G[258]	1705	413.5	18	75
340	G[260]	1684	313.5	18	75
341	G[262]	1663	413.5	18	75
342	G[264]	1642	313.5	18	75
343	G[266]	1621	413.5	18	75
344	G[268]	1600	313.5	18	75
345	G[270]	1579	413.5	18	75
346	G[272]	1558	313.5	18	75
347	G[274]	1537	413.5	18	75
348	G[276]	1516	313.5	18	75
349	G[278]	1495	413.5	18	75
350	G[280]	1474	313.5	18	75
351	G[282]	1453	413.5	18	75
352	G[284]	1432	313.5	18	75
353	G[286]	1411	413.5	18	75
354	G[288]	1390	313.5	18	75
355	G[290]	1369	413.5	18	75
356	G[292]	1348	313.5	18	75

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No.	Name	X-axis	Y-axis	W	H
357	G[294]	1327	413.5	18	75
358	DUMMY[11]	1306	313.5	18	75
359	DUMMY[10]	1285	413.5	18	75
360	VBD[3]	1176.5	420	12	100
361	S_ADDS[0]	1150.5	420	12	100
362	S_ADDS[1]	1137.5	301	12	100
363	S_ADDS[2]	1124.5	420	12	100
364	S_ADDS[3]	1111.5	301	12	100
365	S_ADDS[4]	1098.5	420	12	100
366	S_ADDS[5]	1085.5	301	12	100
367	S_ADDS[6]	1072.5	420	12	100
368	S_ADDS[7]	1059.5	301	12	100
369	VBD[1]	1046.5	420	12	100
370	S[0]	1033.5	301	12	100
371	S[1]	1020.5	420	12	100
372	S[2]	1007.5	301	12	100
373	S[3]	994.5	420	12	100
374	S[4]	981.5	301	12	100
375	S[5]	968.5	420	12	100
376	S[6]	955.5	301	12	100
377	S[7]	942.5	420	12	100
378	S[8]	929.5	301	12	100
379	S[9]	916.5	420	12	100
380	S[10]	903.5	301	12	100
381	S[11]	890.5	420	12	100
382	S[12]	877.5	301	12	100
383	S[13]	864.5	420	12	100
384	S[14]	851.5	301	12	100
385	S[15]	838.5	420	12	100
386	S[16]	825.5	301	12	100
387	S[17]	812.5	420	12	100
388	S[18]	799.5	301	12	100
389	S[19]	786.5	420	12	100
390	S[20]	773.5	301	12	100
391	S[21]	760.5	420	12	100
392	S[22]	747.5	301	12	100
393	S[23]	734.5	420	12	100
394	S[24]	721.5	301	12	100
395	S[25]	708.5	420	12	100
396	S[26]	695.5	301	12	100
397	S[27]	682.5	420	12	100
398	S[28]	669.5	301	12	100
399	S[29]	656.5	420	12	100
400	S[30]	643.5	301	12	100
401	S[31]	630.5	420	12	100
402	S[32]	617.5	301	12	100
403	S[33]	604.5	420	12	100
404	S[34]	591.5	301	12	100
405	S[35]	578.5	420	12	100
406	S[36]	565.5	301	12	100
407	S[37]	552.5	420	12	100
408	S[38]	539.5	301	12	100
409	S[39]	526.5	420	12	100
410	S[40]	513.5	301	12	100
411	S[41]	500.5	420	12	100
412	S[42]	487.5	301	12	100
413	S[43]	474.5	420	12	100
414	S[44]	461.5	301	12	100
415	S[45]	448.5	420	12	100
416	S[46]	435.5	301	12	100

No.	Name	X-axis	Y-axis	W	H
417	S[47]	422.5	420	12	100
418	S[48]	409.5	301	12	100
419	S[49]	396.5	420	12	100
420	S[50]	383.5	301	12	100
421	S[51]	370.5	420	12	100
422	S[52]	357.5	301	12	100
423	S[53]	344.5	420	12	100
424	S[54]	331.5	301	12	100
425	S[55]	318.5	420	12	100
426	S[56]	305.5	301	12	100
427	S[57]	292.5	420	12	100
428	S[58]	279.5	301	12	100
429	S[59]	266.5	420	12	100
430	S[60]	253.5	301	12	100
431	S[61]	240.5	420	12	100
432	S[62]	227.5	301	12	100
433	S[63]	214.5	420	12	100
434	S[64]	201.5	301	12	100
435	S[65]	188.5	420	12	100
436	S[66]	175.5	301	12	100
437	S[67]	162.5	420	12	100
438	S[68]	149.5	301	12	100
439	S[69]	136.5	420	12	100
440	S[70]	123.5	301	12	100
441	S[71]	110.5	420	12	100
442	S[72]	97.5	301	12	100
443	S[73]	84.5	420	12	100
444	S[74]	71.5	301	12	100
445	S[75]	58.5	420	12	100
446	S[76]	45.5	301	12	100
447	S[77]	32.5	420	12	100
448	S[78]	19.5	301	12	100
449	S[79]	6.5	420	12	100
450	S[80]	-6.5	301	12	100
451	S[81]	-19.5	420	12	100
452	S[82]	-32.5	301	12	100
453	S[83]	-45.5	420	12	100
454	S[84]	-58.5	301	12	100
455	S[85]	-71.5	420	12	100
456	S[86]	-84.5	301	12	100
457	S[87]	-97.5	420	12	100
458	S[88]	-110.5	301	12	100
459	S[89]	-123.5	420	12	100
460	S[90]	-136.5	301	12	100
461	S[91]	-149.5	420	12	100
462	S[92]	-162.5	301	12	100
463	S[93]	-175.5	420	12	100
464	S[94]	-188.5	301	12	100
465	S[95]	-201.5	420	12	100
466	S[96]	-214.5	301	12	100
467	S[97]	-227.5	420	12	100
468	S[98]	-240.5	301	12	100
469	S[99]	-253.5	420	12	100
470	S[100]	-266.5	301	12	100
471	S[101]	-279.5	420	12	100
472	S[102]	-292.5	301	12	100
473	S[103]	-305.5	420	12	100
474	S[104]	-318.5	301	12	100
475	S[105]	-331.5	420	12	100
476	S[106]	-344.5	301	12	100

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No.	Name	X-axis	Y-axis	W	H
477	S[107]	-357.5	420	12	100
478	S[108]	-370.5	301	12	100
479	S[109]	-383.5	420	12	100
480	S[110]	-396.5	301	12	100
481	S[111]	-409.5	420	12	100
482	S[112]	-422.5	301	12	100
483	S[113]	-435.5	420	12	100
484	S[114]	-448.5	301	12	100
485	S[115]	-461.5	420	12	100
486	S[116]	-474.5	301	12	100
487	S[117]	-487.5	420	12	100
488	S[118]	-500.5	301	12	100
489	S[119]	-513.5	420	12	100
490	S[120]	-526.5	301	12	100
491	S[121]	-539.5	420	12	100
492	S[122]	-552.5	301	12	100
493	S[123]	-565.5	420	12	100
494	S[124]	-578.5	301	12	100
495	S[125]	-591.5	420	12	100
496	S[126]	-604.5	301	12	100
497	S[127]	-617.5	420	12	100
498	S[128]	-630.5	301	12	100
499	S[129]	-643.5	420	12	100
500	S[130]	-656.5	301	12	100
501	S[131]	-669.5	420	12	100
502	S[132]	-682.5	301	12	100
503	S[133]	-695.5	420	12	100
504	S[134]	-708.5	301	12	100
505	S[135]	-721.5	420	12	100
506	S[136]	-734.5	301	12	100
507	S[137]	-747.5	420	12	100
508	S[138]	-760.5	301	12	100
509	S[139]	-773.5	420	12	100
510	S[140]	-786.5	301	12	100
511	S[141]	-799.5	420	12	100
512	S[142]	-812.5	301	12	100
513	S[143]	-825.5	420	12	100
514	S[144]	-838.5	301	12	100
515	S[145]	-851.5	420	12	100
516	S[146]	-864.5	301	12	100
517	S[147]	-877.5	420	12	100
518	S[148]	-890.5	301	12	100
519	S[149]	-903.5	420	12	100
520	S[150]	-916.5	301	12	100
521	S[151]	-929.5	420	12	100
522	S[152]	-942.5	301	12	100
523	S[153]	-955.5	420	12	100
524	S[154]	-968.5	301	12	100
525	S[155]	-981.5	420	12	100
526	S[156]	-994.5	301	12	100
527	S[157]	-1007.5	420	12	100
528	S[158]	-1020.5	301	12	100
529	S[159]	-1033.5	420	12	100
530	VBD[2]	-1046.5	301	12	100
531	S_ADDE[0]	-1059.5	420	12	100
532	S_ADDE[1]	-1072.5	301	12	100
533	S_ADDE[2]	-1085.5	420	12	100
534	S_ADDE[3]	-1098.5	301	12	100
535	S_ADDE[4]	-1111.5	420	12	100
536	S_ADDE[5]	-1124.5	301	12	100

No.	Name	X-axis	Y-axis	W	H
537	S_ADDE[6]	-1137.5	420	12	100
538	S_ADDE[7]	-1150.5	301	12	100
539	VBD[4]	-1176.5	301	12	100
540	DUMMY[12]	-1285	313.5	18	75
541	DUMMY[13]	-1306	413.5	18	75
542	G[295]	-1327	313.5	18	75
543	G[293]	-1348	413.5	18	75
544	G[291]	-1369	313.5	18	75
545	G[289]	-1390	413.5	18	75
546	G[287]	-1411	313.5	18	75
547	G[285]	-1432	413.5	18	75
548	G[283]	-1453	313.5	18	75
549	G[281]	-1474	413.5	18	75
550	G[279]	-1495	313.5	18	75
551	G[277]	-1516	413.5	18	75
552	G[275]	-1537	313.5	18	75
553	G[273]	-1558	413.5	18	75
554	G[271]	-1579	313.5	18	75
555	G[269]	-1600	413.5	18	75
556	G[267]	-1621	313.5	18	75
557	G[265]	-1642	413.5	18	75
558	G[263]	-1663	313.5	18	75
559	G[261]	-1684	413.5	18	75
560	G[259]	-1705	313.5	18	75
561	G[257]	-1726	413.5	18	75
562	G[255]	-1747	313.5	18	75
563	G[253]	-1768	413.5	18	75
564	G[251]	-1789	313.5	18	75
565	G[249]	-1810	413.5	18	75
566	G[247]	-1831	313.5	18	75
567	G[245]	-1852	413.5	18	75
568	G[243]	-1873	313.5	18	75
569	G[241]	-1894	413.5	18	75
570	G[239]	-1915	313.5	18	75
571	G[237]	-1936	413.5	18	75
572	G[235]	-1957	313.5	18	75
573	G[233]	-1978	413.5	18	75
574	G[231]	-1999	313.5	18	75
575	G[229]	-2020	413.5	18	75
576	G[227]	-2041	313.5	18	75
577	G[225]	-2062	413.5	18	75
578	G[223]	-2083	313.5	18	75
579	G[221]	-2104	413.5	18	75
580	G[219]	-2125	313.5	18	75
581	G[217]	-2146	413.5	18	75
582	G[215]	-2167	313.5	18	75
583	G[213]	-2188	413.5	18	75
584	G[211]	-2209	313.5	18	75
585	G[209]	-2230	413.5	18	75
586	G[207]	-2251	313.5	18	75
587	G[205]	-2272	413.5	18	75
588	G[203]	-2293	313.5	18	75
589	G[201]	-2314	413.5	18	75
590	G[199]	-2335	313.5	18	75
591	G[197]	-2356	413.5	18	75
592	G[195]	-2377	313.5	18	75
593	G[193]	-2398	413.5	18	75
594	G[191]	-2419	313.5	18	75
595	G[189]	-2440	413.5	18	75
596	G[187]	-2461	313.5	18	75

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No.	Name	X-axis	Y-axis	W	H
597	G[185]	-2482	413.5	18	75
598	G[183]	-2503	313.5	18	75
599	G[181]	-2524	413.5	18	75
600	G[179]	-2545	313.5	18	75
601	G[177]	-2566	413.5	18	75
602	G[175]	-2587	313.5	18	75
603	G[173]	-2608	413.5	18	75
604	G[171]	-2629	313.5	18	75
605	G[169]	-2650	413.5	18	75
606	G[167]	-2671	313.5	18	75
607	G[165]	-2692	413.5	18	75
608	G[163]	-2713	313.5	18	75
609	G[161]	-2734	413.5	18	75
610	G[159]	-2755	313.5	18	75
611	G[157]	-2776	413.5	18	75
612	G[155]	-2797	313.5	18	75
613	G[153]	-2818	413.5	18	75
614	G[151]	-2839	313.5	18	75
615	G[149]	-2860	413.5	18	75
616	G[147]	-2881	313.5	18	75
617	G[145]	-2902	413.5	18	75
618	G[143]	-2923	313.5	18	75
619	G[141]	-2944	413.5	18	75
620	G[139]	-2965	313.5	18	75
621	G[137]	-2986	413.5	18	75
622	G[135]	-3007	313.5	18	75
623	G[133]	-3028	413.5	18	75
624	G[131]	-3049	313.5	18	75
625	G[129]	-3070	413.5	18	75
626	G[127]	-3091	313.5	18	75
627	G[125]	-3112	413.5	18	75
628	G[123]	-3133	313.5	18	75
629	G[121]	-3154	413.5	18	75
630	G[119]	-3175	313.5	18	75
631	G[117]	-3196	413.5	18	75
632	G[115]	-3217	313.5	18	75
633	G[113]	-3238	413.5	18	75
634	G[111]	-3259	313.5	18	75
635	G[109]	-3280	413.5	18	75
636	G[107]	-3301	313.5	18	75
637	G[105]	-3322	413.5	18	75
638	G[103]	-3343	313.5	18	75
639	G[101]	-3364	413.5	18	75
640	G[99]	-3385	313.5	18	75
641	G[97]	-3406	413.5	18	75
642	G[95]	-3427	313.5	18	75
643	G[93]	-3448	413.5	18	75
644	G[91]	-3469	313.5	18	75
645	G[89]	-3490	413.5	18	75
646	G[87]	-3511	313.5	18	75

No.	Name	X-axis	Y-axis	W	H
647	G[85]	-3532	413.5	18	75
648	G[83]	-3553	313.5	18	75
649	G[81]	-3574	413.5	18	75
650	G[79]	-3595	313.5	18	75
651	G[77]	-3616	413.5	18	75
652	G[75]	-3637	313.5	18	75
653	G[73]	-3658	413.5	18	75
654	G[71]	-3679	313.5	18	75
655	G[69]	-3700	413.5	18	75
656	G[67]	-3721	313.5	18	75
657	G[65]	-3742	413.5	18	75
658	G[63]	-3763	313.5	18	75
659	G[61]	-3784	413.5	18	75
660	G[59]	-3805	313.5	18	75
661	G[57]	-3826	413.5	18	75
662	G[55]	-3847	313.5	18	75
663	G[53]	-3868	413.5	18	75
664	G[51]	-3889	313.5	18	75
665	G[49]	-3910	413.5	18	75
666	G[47]	-3931	313.5	18	75
667	G[45]	-3952	413.5	18	75
668	G[43]	-3973	313.5	18	75
669	G[41]	-3994	413.5	18	75
670	G[39]	-4015	313.5	18	75
671	G[37]	-4036	413.5	18	75
672	G[35]	-4057	313.5	18	75
673	G[33]	-4078	413.5	18	75
674	G[31]	-4099	313.5	18	75
675	G[29]	-4120	413.5	18	75
676	G[27]	-4141	313.5	18	75
677	G[25]	-4162	413.5	18	75
678	G[23]	-4183	313.5	18	75
679	G[21]	-4204	413.5	18	75
680	G[19]	-4225	313.5	18	75
681	G[17]	-4246	413.5	18	75
682	G[15]	-4267	313.5	18	75
683	G[13]	-4288	413.5	18	75
684	G[11]	-4309	313.5	18	75
685	G[9]	-4330	413.5	18	75
686	G[7]	-4351	313.5	18	75
687	G[5]	-4372	413.5	18	75
688	G[3]	-4393	313.5	18	75
689	G[1]	-4414	413.5	18	75
690	T_LDON5V	-4435	313.5	18	75
691	T_LDON5V	-4456	413.5	18	75
692	T_VCOM	-4477	313.5	18	75
693	T_VCOM	-4498	413.5	18	75
694	T_N18V	-4519	313.5	18	75
695	T_N18V	-4540	413.5	18	75

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13. REVISION HISTORY

Revision	Content	Page	Date
1.0.1	JD79661AA datasheet		2023/06/14
1.0.2	Updated Bump information		2023/06/14
1.0.3	Updated Bump information		2023/06/20
1.0.4	Modify application circuit BS pin (must tie high or low)		2023/07/20

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